Offline, Inductor-less AC Linear Regulator

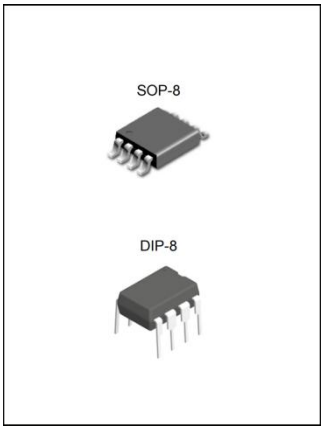
SSP7786

General Description

SSP7786 is a compact, inductor-less, offline linear regulator. It steps down the AC line voltage to 5V, 3.3V and 2.7V by internal. At the same time, VOUT1 can provide a set of 0.66 × VOUT output voltage. It is a simple solution to provide a bias voltage to ICs in offline applications.

SSP7786 integrates a 650V power MOSFET, startup control circuit, VDD voltage control circuit, AC signal synchronization detection circuit, low dropout regulator, etc. The chip integrated smart-control system uses AC line power only when necessary, thus minimizing device losses to achieve good efficiency, and effectively reduce the system standby.

SSP7786 integrates complete protection functions with self-recovery function: VDD Under Voltage Protection, VDD Over Voltage Protection, output Over Load Protection, output Under Voltage Protection, Lightning Surge Protection and built-in Thermal Shutdown Protection.



Features

- High Output Voltage Accuracy: 2%
- Provide Two Sets of Output Voltages simultaneously
- Output Voltage internally Setting
- Smart Control to Maximize Efficiency
- Wide Input Voltage Range: 80~305V AC
- No Power Inductor Required
- No Input High-voltage Capacitor Required
- Fast Line and Load Transient Response
- VDD Under Voltage Protection, VDD Over Voltage Protection
- Short Circuit Protection, Output Under Voltage Protection, Over Load Protection
- Lightning Surge Protection, Built-in Thermal Shutdown Protection
- SOP-8, DIP-8 Package

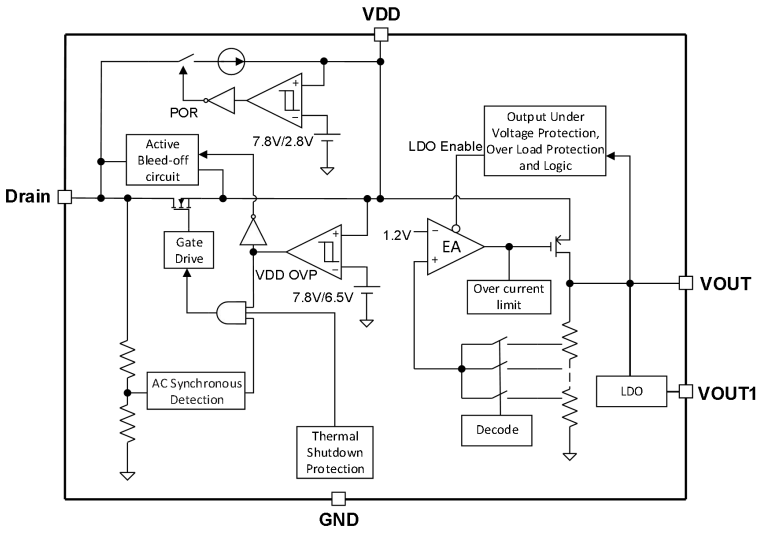
Applications

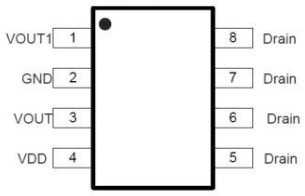
- Smart Meter
- Home Appliance
- Wall Switches and Dimmers

Order specification

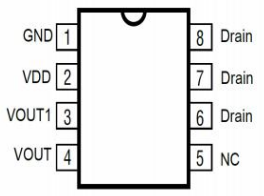
Part No	Package	Manner of Packing	Devices per bag/reel
SSP7786-5V	SOP8	Reel	4000PCS
SSP7786-3.3V	SOP8	Reel	4000PCS
SSP7786-2.7V	SOP8	Reel	4000PCS

Block Diagram and Pin Arrangement Diagram





SOP-8



DIP-8

Pin Assignment

Pin Number		Symbol	Description	Attribute
SOP-8	DIP-8			
1	3	VOT1	LDO output voltage, Vout1=0.66×Vout	O
2	1	GND	Ground.	P
3	4	VOUT	LDO output voltage.	O
4	2	VDD	Voltage input supply, used for energy storage. Connect to GND with a capacitor to transfer the input energy for the LDO output stage.	P
5、6、7、8	6、7、8	Drain	Internal power MOSFET drain pin. Provide energy to the backward stage when the input voltage drops to the charging window interval.	P
-	5	NC	No connected.	-

Functional Description

SSP7786 is a compact, inductor-less, offline linear regulator, can provide two sets of output voltage. SSP7786 integrates 650V power MOSFET, startup control circuit, VDD voltage control circuit, AC signal synchronization detection circuit, low dropout regulator, etc.

Absolute Maximum Ratings

Ta= 25℃, unless specified otherwise.

Parameter	Symbol	Value	Unit
Drain Voltage	V_{Drain}	650	V
VDD Supply Voltage	VDD	9	V
VDD Clamp Current		10	mA
VOUT Voltage	VOUT	-0.3~7	V
Package Thermal Resistance (SOP-8)	$R_{ja(SOP8)}$	165	℃/W
Package Thermal Resistance (DIP-8)	$R_{ja(DIP8)}$	105	℃/W
Maximum Junction Temperature	T_j	150	℃
Operating Temperature Range	T_{amb}	-40~85	℃
Storage Temperature Range	T_{stg}	-65~150	℃
Lead Temperature (Soldering, 10sec.)		260	℃
ESD Capability, HBM (Human Body Model)	HBM	3	KV
ESD Capability, MM (Machine Model)	MM	250	V

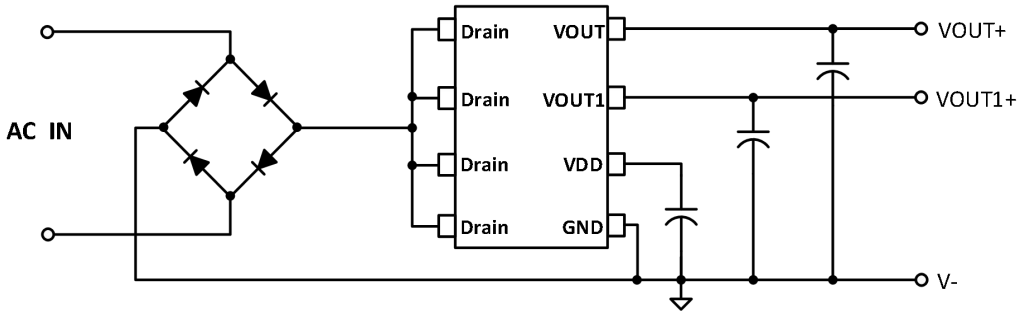
Electrical Characteristics

Ta= 25℃, unless specified otherwise.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Voltage Startup Section (Drain Pin)						
HV Supply Current	I_{HV}	HV=600V, VDD=3V	5	10		mA
HV Leakage Current	$I_{HV\_leakage}$	HV=600V, VDD=8.5V			20	μA
Power MOSFET Drain Source Breakdown Voltage	VBR		650			V
AC Synchronization Turn-off Voltage	VAC_sync_OFF			50		V
Supply Voltage Section（VDD Pin）						

VDD Operating Current	I_{VDD_Op}	Iout=1mA		1.4		mA
VDD Threshold	VDD_ON		7.6	7.8	8	V
VDD Under Voltage Threshold	VDD_OFF			1.2		V
VDD OVP Threshold	VDD_OVP		7.6	7.8	8	V
VDD OVP Threshold Hysteresis	VDD_OVP_hys		6.3	6.5	6.7	V
VOUT Section (VOUT Pin)						
Output Voltage	VOUT_3.3V	Internal setting	3.2	3.3	3.4	V
Output Voltage	VOUT_2.7V	Internal setting	2.65	2.7	2.75	V
Output Voltage	VOUT_5V	Internal setting	4.9	5	5.1	V
Output Voltage	VOUT1	Internal setting		0.66* V_{OUT}		V
Output Current Limit	ILIM		100	138	160	mA
Output Under Voltage Protection	VUVP		10	12.5	15	%
Line Regulation dVout/dVin	ΔVOUT(VIN)	Iout=100μA		0.2		%/V
Power Supply Rejection Ratio	PSRR	Iout=30mA, Cout=4.7μF, f=10Hz to 60KHz		60		dB
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	160	--	℃
Thermal Shutdown Recovery	T_{RC}			140	--	℃

Application Circuits



Startup Current

During the start-up phase of the SSP7786, the internal high voltage current source(10mA) charges the VDD capacitor though the Drain pin. The charging current stops when the VDD voltage rises to VDD_ON while the IC starts to work normally. The main power channel is switched from the high-voltage current source to provide energy for the internal power MOSFET pair to the later stage.

AC Synchronous detection with Active Bleed-off Circuit

SSP7786 is integrated with AC synchronous detection circuit, the circuit through the Drain end to ground built-in voltage divider resistor AC signal detection. When the chip detects that the Drain voltage is below VAC_sync_OFF, the internal power MOSFET is turned on to charge the VDD capacitor.

The Drain voltage may not enter its charging window during normal operation due to parasitic capacitance from Drain to GND. To solve this problem, an active bleeder circuit is designed inside the chip. The drain circuit opens the drain channel of the internal drain-VDD when the VDD voltage is lower than VDD_OVP_hys, and closes the drain channel when the VDD voltage reaches VDD_OVP. The active bleeder control of the parasitic capacitance at the drain end of the chip ensures that enough input energy can be used to charge the VDD during the charging window. In addition, when various kinds of protection (UVP, OLP or OTP) occur, the active discharge circuit will also be opened to charge the VDD capacitor and discharge the parasitic capacitor at the Drain end, so as to ensure the smooth development of the subsequent protection logic and the smooth progress of the self-recovery restart.

Output current limit

SSP7786 has integrated output current limiting circuit. The circuit detects the output current of the LDO and directly controls the on-off of the LDO. To avoid chip damage caused by excessive LDO output current when short circuit or overload occurs, the typical output current limit is set to 138mA. In the event of a short circuit or overload, the circuit limits the maximum output current and triggers output undervoltage protection with output voltage sags. Here the output current is the sum of the current of the two outputs of VOUT and VOUT1.

Output Under Voltage Protection (UVP)

When the output power is greater than the maximum power that the SSP7786 can provide, the output voltage will sag. When the output voltage sag value exceeds 12.5% of its rated voltage, the output under voltage protection is triggered, and the LDO shuts down and waits for two AC cycles before restarting.

Over Load Protection (OLP)

As the load increases, the output voltage decreases, and the system triggers the output under voltage protection. When the SSP7786 continuously triggers the under voltage protection for more than 50ms, the system triggers the overload protection, turns off the internal power MOSFET and LDO output, and starts the self-recovery restart process after 640ms self-recovery delay time. At the same time, the VDD voltage is pulled up to the VDD_OVP by an internal high-voltage current source.

VDD Over Voltage Protection (VDD OVP)

After starting, SSP7786 turns on VDD over voltage protection function. During the AC charging window, the VDD voltage has 2 behavior modes. One is when the VDD voltage rises to the OVP trigger voltage (typical 7.8V) during the current charging window, then the SSP7786 turns off the internal power MOSFET and limits the maximum VDD voltage. The other is that the VDD cannot rise to the OVP trigger point during the current charging window, then the internal power MOSFET is turned off by the AC synchronization detection signal and waits for the next charging window to continue charging. In this way, the AC AC input energy is transferred only in the low-voltage part of the main line, thus reducing the loss of the internal power MOSFET. When the internal power MOSFET is turned on, the input current provides energy to the VDD capacitor and load. When the MSOFET is off, the load is supplied with energy by the VDD capacitor discharge.

The following formula is recommended to calculate the VDD capacitance：

$$Cvdd \approx 0.01 \times Iload \quad （unit=F）$$

Lightning Surge Protection

When a lightning surge occurs, the AC line voltage couples a very high surge spike. If the surge spike occurs during the SSP7786 charging window and exceeds 100Vdc in amplitude, the system triggers lightning surge protection and the IC quickly shuts down the internal power MOSFET until the surge spike decreases. During the surge, the IC outputs continuously.

Built-in Thermal Shutdown (OTP)

When the chip temperature exceeds 160℃, the chip triggers the over-temperature protection to turn off the main power MOSFET and LDO output. When the temperature falls below its lower threshold of 140℃, the chip is enabled again.

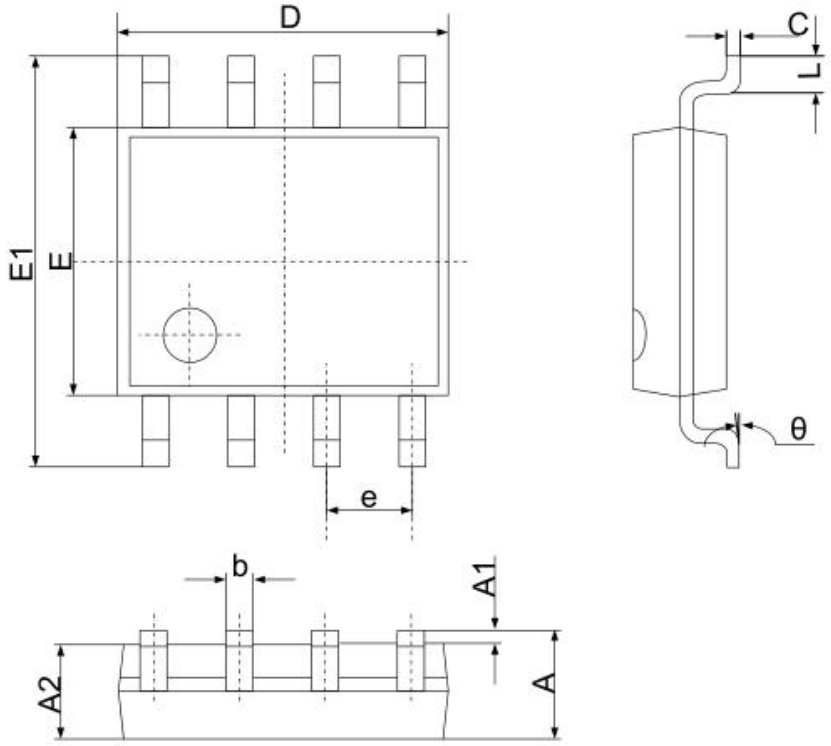
Self-recovery restart

Upon triggering various protections, such as OLP and OTP, the chip will enter a self-recovery restart process, while the power MOSFET inside the chip is turned off. After the 640ms self-recovery delay time, the internal signal of the chip is reset and restarted. Then, if the protection state still exists, the chip continues to repeat the above self-recovery restart action.

PCB Layout Guidelines:

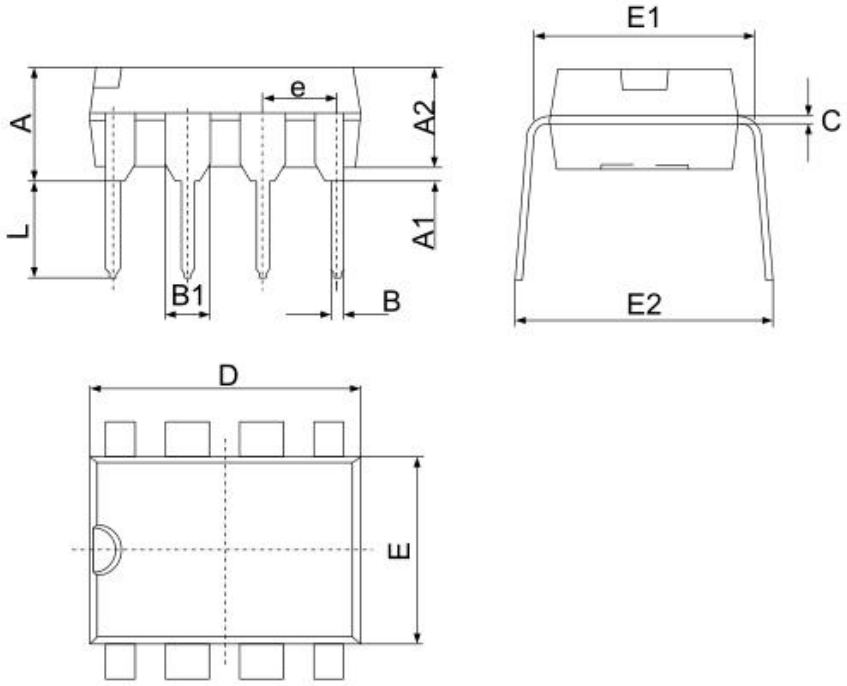
Connect 5,6,7, and 8 pins together and maximize the area to facilitate heat dissipation.

Package Information（SOP8）



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information（DIP8）



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354

Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version：V1.1	Author：Yang	Time：2021.9.27
Modify the record：		
1. Re-typesetting the manual and checking some data		
Version：V1.2	Author：Yang	Time：2024.5.9
Modify the record：		
1. Modifying the Application Circuits		

Statement

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