

Dual-key Touch Sensor IC

SSP8012

General Description

The SSP8012 is a low-power dual-key touch sensor IC. The operating mode is divided into Normal mode and Low Power mode.



Features

- Dual-key Sensor IC
- Operation Voltage: 2.2V~5.5V
- Operation Current: Normal mode = 3.6μA/Low Power mode = 1.7μA @VDD=3V
- Operating mode divided into Normal mode and Low Power mode. Enter Low Power mode after no activity for 12 second
- Response Time: Normal mode < 70mS; Low Power mode < 140mS
- Sensitivity adjusted by Key pin capacitor(0pF~30pF)
- Selectable output level: Active High or Active Low or Open Drain Output
- Key press timeout reset: 10 seconds
- Built-in 2.3V LDO
- SOT23-6, package

Applications

- Household appliance
- Intelligent instrument

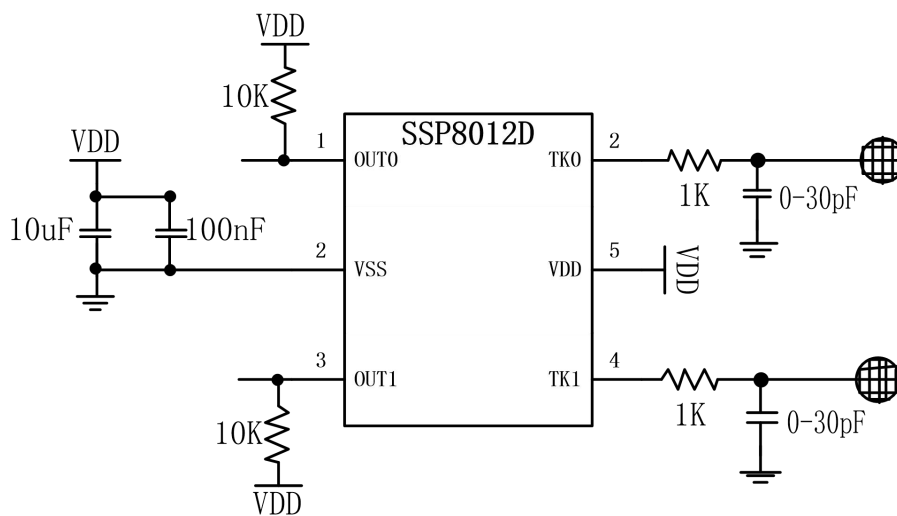
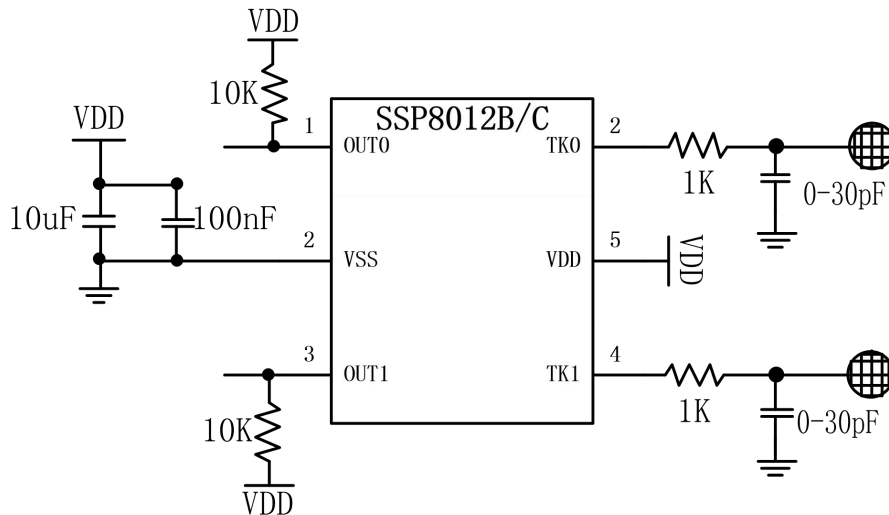
Order specification

Part No	Package	Manner of Packing	Devices per bag/reel
SSP8012B	SOT23-6	Reel	3000
SSP8012C	SOT23-6	Reel	3000
SSP8012D	SOT23-6	Reel	3000

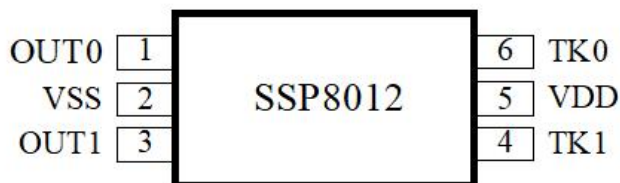
Selection Table

Part No	Key press timeout reset	OUT level	Sensitivity	2.3V LDO
SSP8012B	10 seconds	CMOS output Active High	High	ON
SSP8012C	10 seconds	CMOS output Active Low	High	ON
SSP8012D	10 seconds	Open-drain output Active-low	High	ON

Application Circuits



Pin Arrangement Diagram



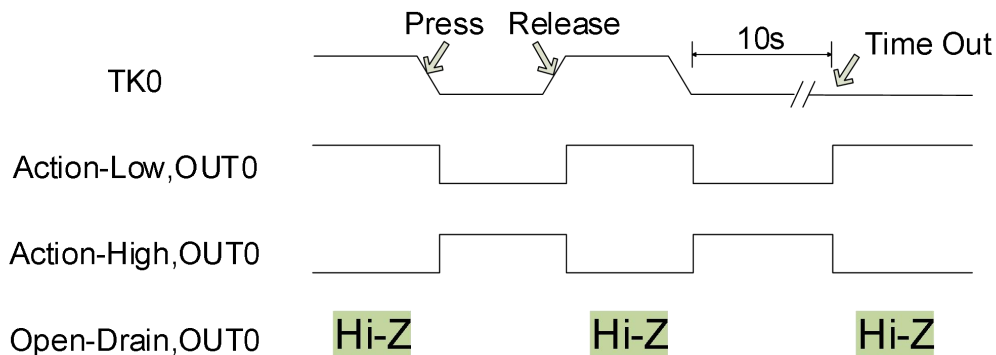
SSP8012B/C/D(SOT23-6) Pin Assignment

No.	Name	In/Out	Pin Description
1,3	OUT0, OUT1	O	Output state
2	VSS	G	Ground
4,6	TK0, TK1	I	Capacitive Touch Sensor Input.Key pin capacitor adjust sensitivity(0pF~30pF)
5	VDD	P	Power input pin

Functional Description

1.Output Pin Mode Selection

OUT0 and OUT1 are button output modes. Their output levels are determined by the chip model and can be selected as: Active High,Active Low,Open-drain output



2.Touch Sensitivity Adjustment

The sensitivity of touch key can be adjusted by the capacitance of Key pin. The adjustment range is from 0pF to 30pF. Smaller capacitance can make higher sensitivity.

3.Key Press Timeout Reset

Long press on the touch key will produce a timeout reset. The maximum time is 10 seconds.

4.Normal mode and Low Power mode

After the chip is reset, enter the normal mode to work. When 12 seconds have no touch event,

it enters the low-power mode. When the chip detects the capacitor change of the TK pin, it will return from low power mode to normal mode.

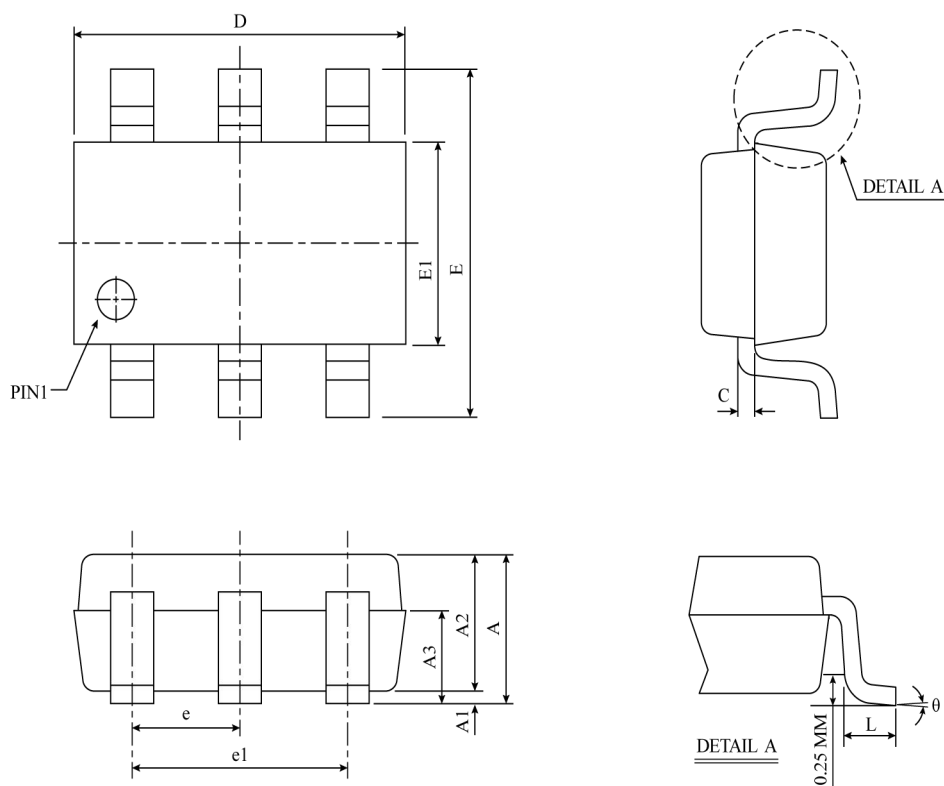
Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage	V_{DD}	$V_{SS}-0.3 \sim V_{SS}+5.5$	V
Input voltage	V_{IN}	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Operating temperature	T_{amb}	$-20 \sim +70$	°C
Storage temperature	T_{stg}	$-65 \sim +150$	°C

Electrical Characteristics($T_a=25^{\circ}\text{C}$)

Parameter	Sym bol	Test Conditions		Min.	Typ.	Max.	Uni t
Operating voltage	VDD	-		2.2	-	5.5	V
I/O Port Source Current	IOH	all Output	VDD=3.0V VOH=2.7V	-	5	-	mA
			VDD=5.0V VOH=4.5V	-	10	-	mA
I/O Port Sink Current	IOL	all Output	VDD=3.0V VOL=0.3V	-	15	-	mA
			VDD=5.0V VOL=0.5V	-	30	-	mA
Power Supply Current	IDD	Normal mode	VDD=4.2V	-	4.2	-	μA
			VDD=3.6V	-	3.7	-	μA
			VDD=3.0V	-	3.6	-	μA
		Low Power mode	VDD=4.2V	-	2.1	-	μA
			VDD=3.6V	-	1.8	-	μA
			VDD=3.0V	-	1.7	-	μA
Timeout Lead Time	TLT	VDD=3.0V		-	10	-	S
Enter Low Power mode after no activity time	Tr	VDD=3.0V		-	12	-	S
Normal mode Response Time	t	VDD=3.0V		50	60	70	ms
Low Power mode Response Time	t	VDD=3.0V		50	120	140	ms
LVR Voltage	VLVR	TA=25°C		1.8	1.9	2.1	V

Package Information (SOT23-6)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.45	-	-	0.057
A1	0	0.08	0.15	0	0.003	0.006
A2	0.90	1.10	1.30	0.035	0.043	0.051
A3	0.60	0.65	0.70	0.024	0.026	0.028
c	0.12	0.16	0.19	0.005	0.006	0.007
D	2.82	2.92	3.02	0.111	0.115	0.119
E	2.70	2.90	3.10	0.106	0.114	0.122
E1	1.52	1.62	1.72	0.060	0.064	0.068
e	0.85	0.95	1.05	0.033	0.037	0.041
e1	1.80	1.90	2.00	0.071	0.075	0.079
L	0.35	0.48	0.60	0.014	0.019	0.024
θ	0°	4°	8°	0°	4°	8°
JEDEC	MO-178(AB)					

Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version: V1.0

Author: Chen Yang

Time: 2024.5.9

Modify the record:

1. Editio princeps

Statement

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