# Shanghai Siproin Microelectronics Co.,Ltd.

# Energy Metering IC
# with On-Chip Fault Detection

# SSP1851 DATASHEET

Date：2024/1/8

Version：1.1

Official Website：http://WWW.SIPROIN.COM

# Catalog

## 1.General Description

The SSP1851 is a high-accuracy, fault-tolerant electrical energy measurement IC that is intended for use with 2-wire distribution systems. The part specifications surpass the accuracy requirements as quoted in the IEC1036 standard.

The only analog circuitry used in the SSP1851 is in the ADCs and reference circuit. All other signal processing (e.g., multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

The SSP1851 incorporates a novel fault detection scheme that warns of fault conditions and allows the SSP1851 to continue accurate billing during a fault event. The SSP1851 does this by continuously monitoring both the phase and neutral (return) currents. A fault is indicated when these currents differ by more than 12.5%. Billing is continued using the larger of the two currents.

The SSP1851 supplies average real power information on the low-frequency outputs F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or interface to an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes.

The SSP1851 includes a power supply monitoring circuit on the AVDD supply pin. The SSP1851 will remain in a reset condition until the supply voltage on AVDD reaches 4 V. If the supply falls below 4 V, the SSP1851 will also be reset and no pulses will be issued on F1, F2, and CF. Internal phase matching circuitry ensures that the voltage and current channels are matched whether the HPF in Channel 1 is on or off. The SSP1851 also has anticreep protection.

The SSP1851 is available in 24-lead DIP and SSOP packages.

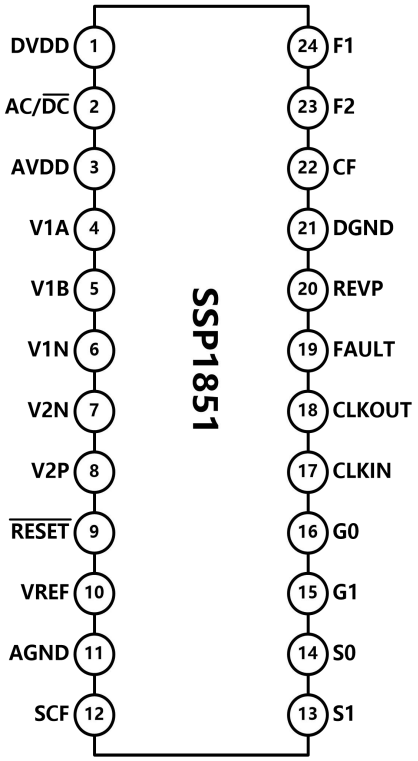
## 2.Features

- High Accuracy, Surpasses 50 Hz/60 Hz IEC 687/1036.Less than 0.1% Error over a Dynamic Range of 500 to 1
- Supplies Average Real Power on the Frequency Outputs F1 and F2
- High-Frequency Output CF Is Intended for Calibration and Supplies Instantaneous Real Power
- Continuous Monitoring of the Phase and Neutral Current Allows Fault Detection in 2-Wire Distribution Systems
- SSP1851 Uses the Larger of the Two Currents (Phase or Neutral) to Bill—Even During a Fault Condition
- Two Logic Outputs (FAULT and REVP) Can Be Used to Indicate a Potential Miswiring or Fault Condition
- Direct Drive for Electromechanical Counters and 2-Phase Stepper Motors (F1 and F2)
- A PGA in the Current Channel Allows the Use of Small Values of Shunt and Burden Resistance
- Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time
- On-Chip Power Supply Monitoring
- On-Chip Creep Protection (No Load Threshold)
- On-Chip Reference 2.5 V ±8% (30 ppm/°C Typical) with External Overdrive Capability
- chip contains a highly stable oscillator with little sensitivity to temperature
- Single 5 V Supply, Low Power (15 mW Typical)
- Low-Cost CMOS Process

## 3.Order specification

| Part No | Package | Manner of Packing | Devices per bag/reel |
|---|---|---|---|
| SSP1851-SSOP24 | SSOP24 | Reel | 2500PCS |

## 4.Pin Assignment




SSOP24

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | DVDD | Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the SSP1851. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 2 | AC/$\overline{DC}$ | High-Pass Filter Select. This logic input is used to enable the HPF in Channel 1 (the current channel). A Logic 1 on this pin enables the HPF. The associated phase response of this filter has been internally compensated over a frequency range of 45 Hz to 1 kHz. The HPF filter should be enabled in energy metering applications. |
| 3 | AVDD | Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the SSP1851. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |

| | | |
|---|---|---|
| 4, 5 | V1A, V1B | Analog Inputs for Channel 1 (Current Channel). These inputs are fully differential voltage inputs with a maximum signal level of ±660 mV with respect to pin V1N for specified operation. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry and an overvoltage of ±6 V can also be sustained on these inputs without risk of permanent damage. |
| 6 | V1N | Negative Input Pin for Differential Voltage Inputs V1A and V1B. The maximum signal level at this pin is ±1 V with respect to AGND. The input has internal ESD protection circuitry and an overvoltage of ±6 V can also be sustained without risk of permanent damage. This input should be directly connected to the burden resistor and held at a fixed potential, i.e., AGND. See Analog Input section. |
| 7，8 | V2N，V2P | Negative and Positive Inputs for Channel 2 (Voltage Channel). These inputs provide a fully differential input pair. The maximum differential input voltage is ±660 mV for specified operation. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry and an overvoltage of ±6 V can also be sustained on these inputs without risk of permanent damage. |
| 9 | $\overline{\text{RESET}}$ | Reset Pin for the SSP1851. A logic low on this pin will hold the ADCs and digital circuitry in a reset condition. Bringing this pin logic low will clear the SSP1851 internal registers. |
| 10 | REFIN/OUT | Provides Access to the On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.5 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 10 µF ceramic capacitor and 100 nF ceramic capacitor. |
| 11 | AGND | Provides the Ground Reference for the Analog Circuitry in the SSP1851, i.e., ADCs and Reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, e.g., antialiasing filters, current and voltage transducers, and more. For good noise suppression, the analog ground plane should only be connected to the digital ground plane at one point. A star ground configuration will help to keep noisy digital return currents away from the analog circuits. |
| 12 | SCF | Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table IV shows how the calibration frequencies are selected(see Table IV). |
| 13，14 | S1，S0 | These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. See Selecting a Frequency for an Energy Meter Application section(see Table II) . |
| 15，16 | G1，G0 | These logic inputs are used to select one of four possible gains for the analog inputs V1A and V1B. The possible gains are 1, 2, 8, and 16. See Analog Inputs section(see Table I). |

| | | |
|---|---|---|
| 17 | CLKIN | An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the SSP1851. The clock frequency for specified operation is 3.579545 MHz. Crystal load capacitors of between 22 pF and 33 pF (ceramic) should be used with the gate oscillator circuit. |
| 18 | CLKOUT | A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the SSP1851. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN or by the gate oscillator circuit. |
| 19 | FAULT | This logic output will go active high when a fault condition occurs. A fault is defined as a condition under which the signals on V1A and V1B differ by more than 12.5%. The logic output will be reset to zero when a fault condition is no longer detected. See Fault Detection section. |
| 20 | REVP | This logic output will go logic high when negative power is detected, i.e., when the phase angle between the voltage and current signals is greater that 90°. This output is not latched and will be reset when positive power is once again detected. The output will go high or low at the same time as a pulse is issued on CF. |
| 21 | DGND | This provides the ground reference for the digital circuitry in the SSP1851, i.e., multiplier, filter, and digital-to-frequency converter. This pin should be tied to the analog ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, e.g., counters (mechanical and digital), MCUs, and indicator LEDs. For good noise suppression, the analog ground plane should only be connected to the digital ground plane at one point, e.g., a star ground. |
| 22 | CF | Calibration Frequency Logic Output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. Also see SCF pin description(see Table IV ). |
| 23，24 | F2，F1 | Low-Frequency Logic Outputs. F1 and F2 supply average real power information. The logic outputs can be used to directly drive electromechanical counters and 2-phase stepper motors. |

## 5.Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | VDD | -0.3～+7 | V |
| Analog Input Voltage to AGND | V1A,V1B,V1N,V2N,V2P | -6～+6 | V |
| Reference Input Voltage to AGND | | -0.3～VDD+0.3 | V |
| Digital Input Voltage to DGND | | -0.3～VDD+0.3 | V |
| Digital Output Voltage to DGND | | -0.3～VDD+0.3 | V |
| Operating Temperature Range | T | -40～+85 | ℃ |
| Storage Temperature Range | T | -40～+85 | ℃ |
| Junction Temperature | T | +150 | ℃ |
| SSOP24 Power Dissipation | Pd | 450 | mW |
| Thermal Impedance | | 112 | ℃/W |

| | | | |
|---|---|---|---|
| Lead Temperature, Soldering Vapor Phase (60 sec) | | +215 | ℃ |
| Infrared (15 sec) | | +220 | ℃ |

Note: TA = 25°C, unless otherwise noted.

## 6.Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 4.75 | 5 | 5.25 | V |
| Operating Current | $I_{DD}$ | | | 3 | 4 | mA |
| Measurement Error[1] on Channels 1 | | Channel 2 with Full-Scale Signal (±660 mV), +25℃, G=1, Dynamic Range 500 to 1 | | 0.1 | | % |
| | | Channel 2 with Full-Scale Signal (±660 mV), +25℃, G=1, Dynamic Range 500 to 1 | | 0.1 | | % |
| Phase Error[1] between Channels | | Line Frequency = 45 Hz to 65 Hz, $AC/\overline{DC}$ =0 and $AC/\overline{DC}$ =1, V1 Phase Lead 37° (PF = 0.8 Capacitive) | | ±0.1 | | % |
| | | Line Frequency = 45 Hz to 65 Hz, $AC/\overline{DC}$ =0 and $AC/\overline{DC}$ =1, V1 Phase Lag 60° (PF = 0.5 Inductive) | | ±0.1 | | % |
| AC Power Supply Rejection Output Frequency Variation (CF) | | $AC/\overline{DC}$ =1, S0=S1=1, G0=G1=0， V1=V2=100mVrms, 50Hz, Ripple on AVDD of 200 mV rms @ 100 Hz | | 0.2 | | % |
| DC Power Supply Rejection Output Frequency Variation (CF) | | $AC/\overline{DC}$ =1, S0=S1=1, G0=G1=0, V1=V2=100mVrms, VDD =5V±250mV | | ±0.3 | | % |
| FAULT DETECTION Fault Detection Threshold | | V1A or V1B Active | | 12.5 | | % |
| FAULT DETECTION Input Swap Threshold | | V1A or V1B Active | | 14 | | % |
| Accuracy Fault Mode Operation | | V1A Active，V1B=AGND，Dynamic Range 500 to 1 | | 0.1 | | % |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | V1B Active，V1A=AGND，Dynamic Range 500 to 1 | | 0.1 | | % |
| Accuracy Fault Mode Operation | | | | 3 | | S |
| Accuracy Fault Mode Operation | | | | 3 | | S |
| **ANALOG INPUTS** | | | | | | |
| Maximum Signal Levels | | V1P,VIN,V2N and V2P to AGND | | | ±1 | V |
| Input Impedance | | CLKOSC=3.58MHz | 390 | | | kΩ |
| -3dBBandwidth | | CLKOSC/256, CLKOSC=3.58MHz | | 14 | | KHZ |
| ADC Offset Error | | | | | ±16 | mV |
| Gain Error | | External 2.5V, G=1<br>V1=660mVdc, V2=660mV dc | | ±5 | ±8 | % |
| Gain Error Match | | External 2.5V | | ±0.2 | | % |
| **REFERENCE INPUT** | | | | | | |
| REFIN/OUT Input Voltage Range | | | 2.3 | 2.5 | 2.7 | V |
| Input Impedance | | | 3.2 | | | kΩ |
| Input Capacitance | | | | | 10 | pF |
| **ON-CHIP REFERENCE** | | | | | | |
| Reference Error | | Nominal 2.5V | | | ±200 | mV |
| Temperature Coefficient | | Nominal 2.5V | | ±30 | | ppm/℃ |
| **CLKIN** | | | | | | |
| Internal Clock Frequency | | Note All Specifications for CLKIN of 3.58MHz | 1 | | 4 | MHZ |
| **LOGIC INPUTS**<br>**SCF，S0，S1，** AC/$\overline{DC}$ **，** $\overline{RESET}$**，G0and G1** | | | | | | |
| Input High Voltage | $V_{INH}$ | VDD=5V±5% | 2.4 | | | |
| Input Low Voltage | $V_{INL}$ | VDD=5V±5% | | | 0.8 | |
| Input Current | | $V_{IN}$=0Vto VDD | | 0.01 | ±3 | uA |
| Input Capacitance | | | | | 10 | pF |
| **LOGIC OUTPUTS**<br>**F1，F2** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$=10mA, VDD=5V | 4.5 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$=10mA, VDD=5V | | | 0.5 | V |
| **CF，REVP** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$=10mA, VDD=5V | 4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$=10mA, VDD=5V | | | 0.5 | V |

Note: TA = 25°C, unless otherwise noted.All voltage values use GND terminal potential as a reference point.

VDD= 5V±5%，GND=0V, On-Chip Reference, CLKOSC=3.58MHz .

# 7.Analog Inputs

## 7.1 Channel V1 (Current Channel)

The voltage outputs from the current transducers are connected to the SSP1851 here. Channel V1 has two voltage inputs, namely V1A and V1B. These inputs are fully differential with respect to V1N. However, at any one time, only one is selected to perform the power calculation.

The analog inputs V1A, V1B, and V1N have the same maximum signal level restrictions as V2P and V2N. However, Channel 1 has a programmable gain amplifier (PGA) with user-selectable gains of 1 to 2, 8, or 16 (see Table I). These gains facilitate easy transducer interfacing.

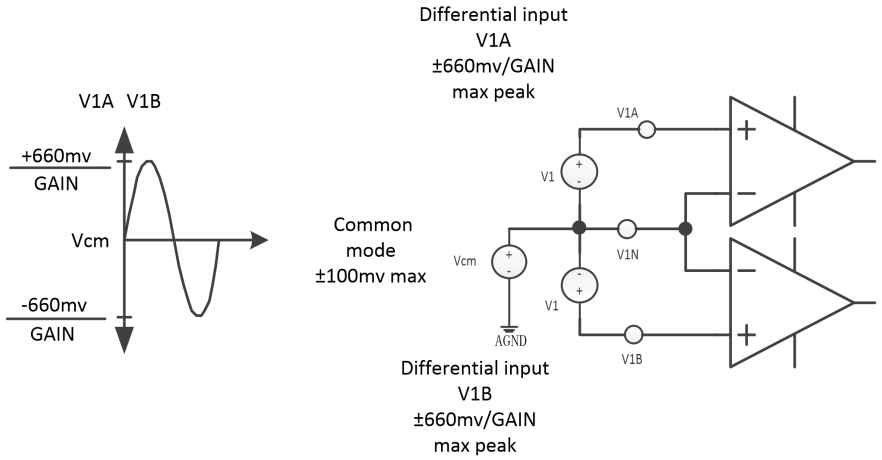



*Figure 1. Maximum Signal Levels, Channel 1（G=1）*

Figure 1 illustrates the maximum signal levels on V1A, V1B, and V1N. The maximum differential voltage is ±660 mV divided by the gain selection. Again, the differential voltage signal on the inputs must be referenced to a common mode, e.g., AGND. The maximum common-mode signal is ±100 mV as shown in Figure 1.

## 7.2 Channel V2 (Voltage Channel)

The output of the line voltage transducer is connected to the SSP1851 at this analog input. Channel V2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ± 660 mV. Figure 2 illustrates the maximum signal levels that can be connected to the SSP1851 Channel 2.

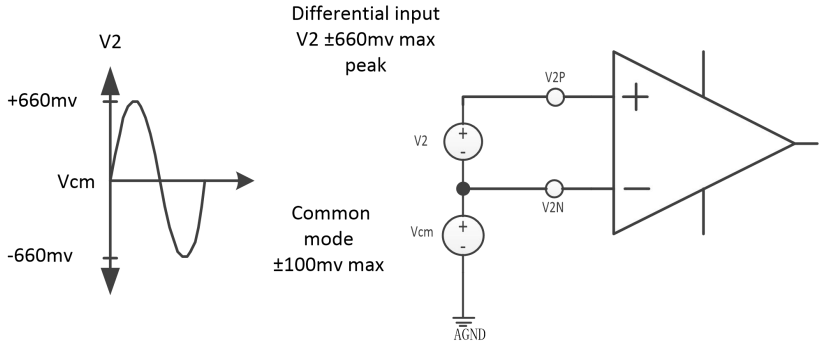



*Figure 2. Maximum Signal Levels, Channel 2*

Channel 2 must be driven from a common-mode voltage, i.e., the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the SSP1851 can be driven with common-mode voltages of up to 100 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

## 8. Typical Connection Diagrams

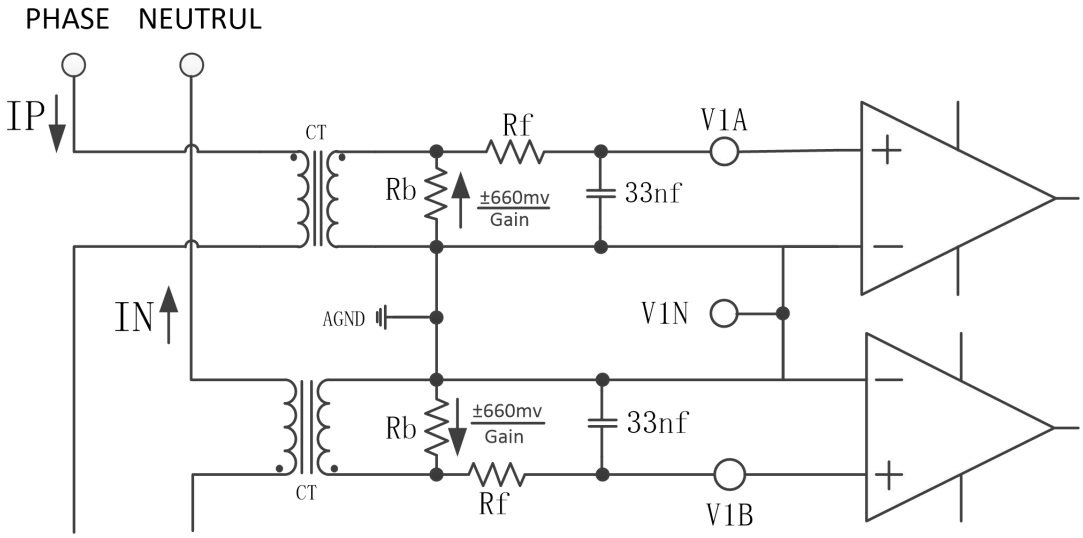



*Figure 3. Typical Connection for Channel 1*

Figure 3 shows a typical connection diagram for Channel V1. Here the analog inputs are being used to monitor both the phase and neutral currents. Because of the large potential difference between the phase and neutral, two CTs (current transformers) must be used to provide the isolation. Notice both CTs are referenced to AGND (analog ground), hence the common-mode voltage is 0 V. The CT turns ratio and burden resistor (Rb) are selected to give a peak differential voltage of ±660 mV/Gain.

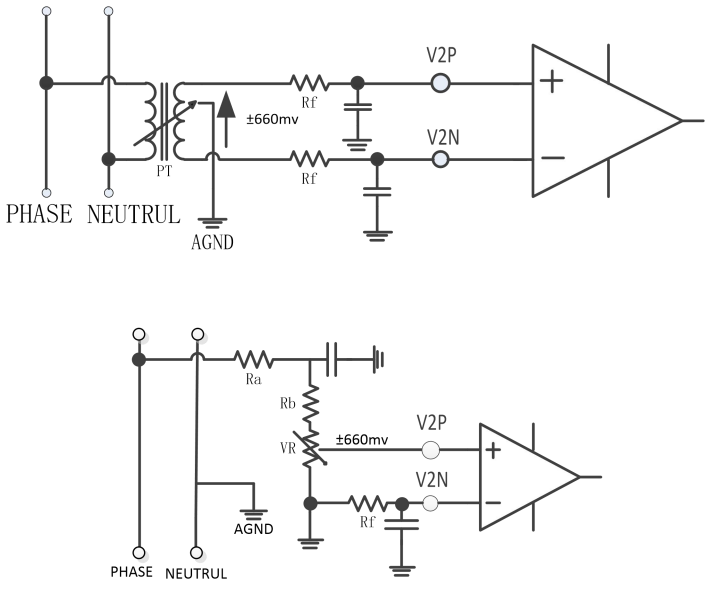



*Figure 4. Typical Connections for Channel 2*

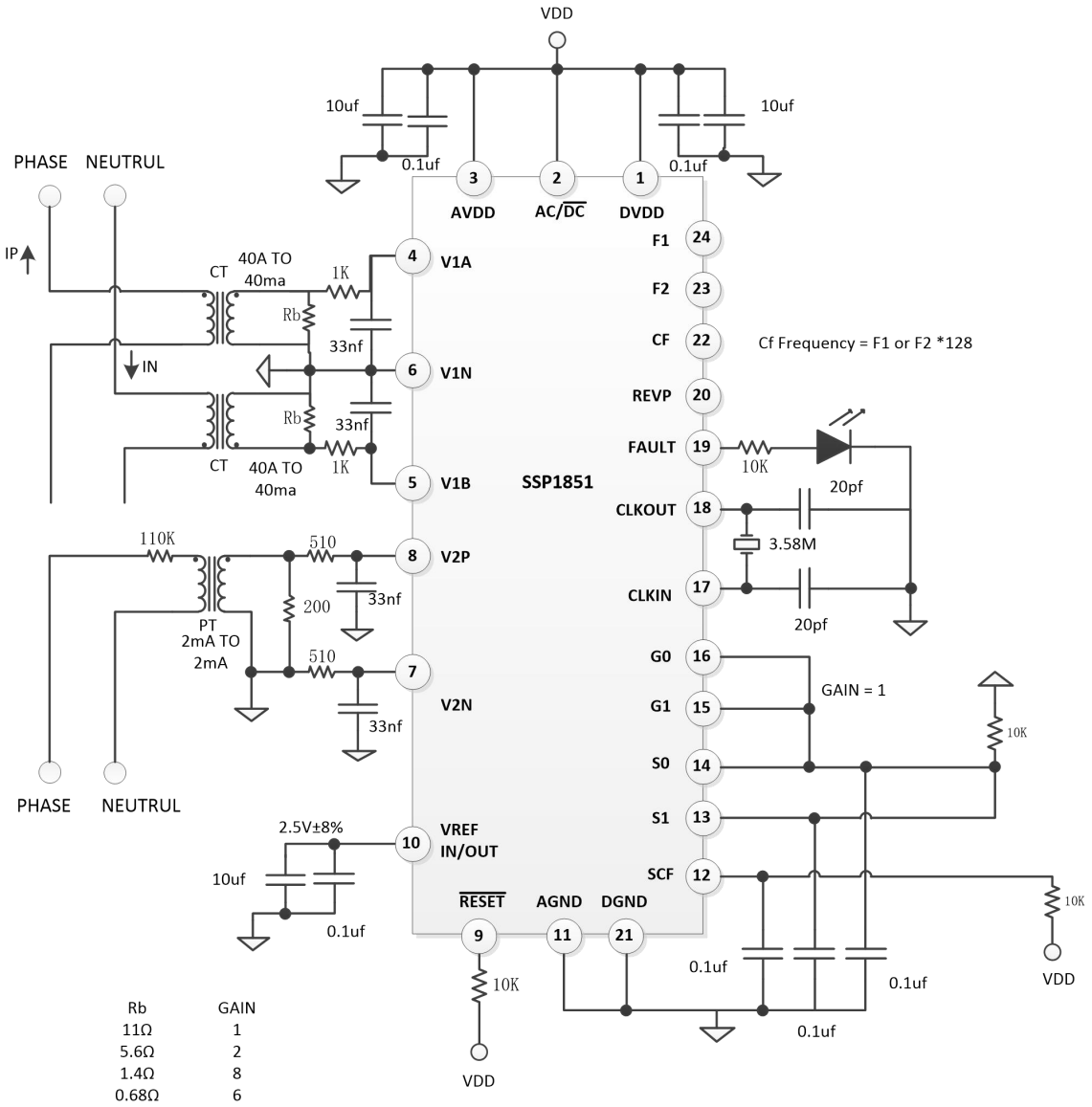
Figure 4 shows two typical connections for Channel V2. The first option uses a PT (potential transformer) to provide complete isolation from the mains voltage. In the second option, the SSP1851 is biased around

the neutral wire and a resistor divider is used to provide a voltage signal that is proportional to the line voltage. Adjusting the ratio of Ra and Rb is also a convenient way of carrying out a gain calibration on the meter.

**Table I Gain Selection for Channel 1**

| G1 | G0 | Gain | Maximum Differential Signal |
|---|---|---|---|
| 0 | 0 | 1 | ±660mv |
| 0 | 1 | 2 | ±330mv |
| 1 | 0 | 8 | ±82mv |
| 1 | 1 | 16 | ±41mv |

## 9. Typical application diagram



### Frequency Outputs F1 and F2

The SSP1851 calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, e.g., 0.34 Hz maximum for ac signals with S0 = S1 = 0 (see Table III). This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The averaging of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation.

$$Freq = \frac{5.74 * V1 * V2 * Gain * \mathrm{F1-4}}{VREF^2}$$

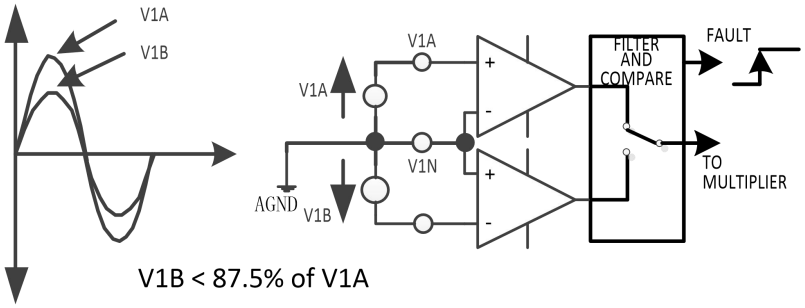
Freq = Output frequency on F1 and F2 (Hz)
V1 = Differential rms voltage signal on Channel 1 (Volts)
V2 = Differential rms voltage signal on Channel 2 (Volts)
Gain = 1, 2, 8, or 16, depending on the PGA gain selection made using logic inputs G0 and G1(see Table I)
VREF = The reference voltage (2.5 V ± 8%) (Volts)
F1–4 = One of four possible frequencies selected by using the logic inputs S0 and S1 (see Table II)

## 10. Fault Detection

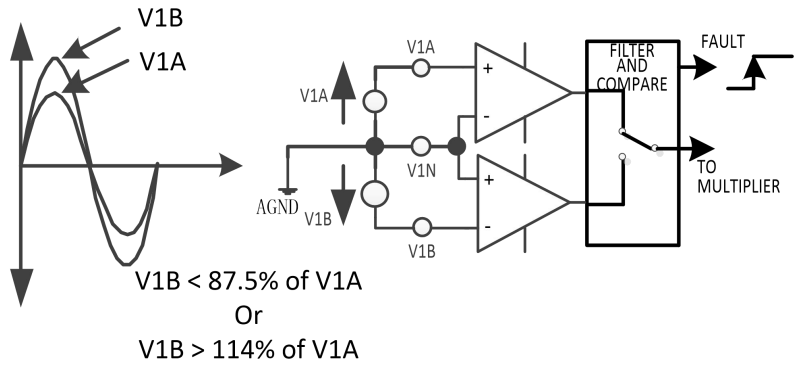
The SSP1851 incorporates a novel fault detection scheme that warns of fault conditions and allows the SSP1851 to continue accurate billing during a fault event. The fault detection function is designed to work over a line frequency of 45 Hz to 55 Hz. The SSP1851 does this by continuously monitoring both the phase and neutral (return) currents. A fault is indicated when these currents differ by more than 12.5%. However, even during a fault, the output pulse rate on F1 and F2 is generated using the larger of the two currents. Because the SSP1851 looks for a difference between the signals on V1A and V1B, it is important that both current transducers are closely matched.

On power-up the output pulse rate of the SSP1851 is proportional to the product of the signals on Channel V1A and Channel 2. If there is a difference of greater than 12.5% between V1A and V1B on power-up, the fault indicator (FAULT) will go active after about one second. In addition, if V1B is greater than V1A the SSP1851 will select V1B as the input. The fault detection is automatically disabled when the voltage signal on Channel 1 is less than 0.5% of the full-scale input range. This will eliminate false detection of a fault due to noise at light loads.

### 10.1 Fault with V1A Greater than V1B




### 10.2 Fault with V1B Greater than V1A




## 11. Frequency Outputs

**Table II Selecting a Frequency of F1-4（CLKOSC=3.579MHz）**

| S1 | S0 | $F_{1-4}$ (Hz) | Prescaling |
|---|---|---|---|
| 0 | 0 | 1.7 | $2^{21}$ |
| 0 | 1 | 3.4 | $2^{20}$ |
| 1 | 0 | 6.8 | $2^{19}$ |
| 1 | 1 | 13.6 | $2^{18}$ |

In this example, if ac voltages of ±660 mV peak are applied to V1 and V2, the expected output frequency is calculated as follows.

Gain = 1, G0 = G1 = 0

F1–4= 1.7 Hz, S0 = S1 = 0

V1 = rms of 660 mV peak ac = 0.66/√2 V

V2 = rms of 660 mV peak ac = 0.66/√2 V

VREF = 2.5 V (nominal reference value)

Note: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = \frac{5.74*0.66/\sqrt{2}*0.66/\sqrt{2}*1*1.7}{2.5^2} = 0.34\ HZ$$

As shown in these two example calculations, the maximum output frequency for ac inputs is always half of that for dc input signals. Table III shows a complete listing of all maxi mum output frequencies.

**Table III Maximum Output Frequency on F1 and F2**

| S1 | S0 | Max Output Frequency | |
|---|---|---|---|
| | | DC Inputs(Hz) | AC Inputs(Hz) |
| 0 | 0 | 0.68 | 0.34 |
| 0 | 1 | 1.36 | 0.68 |
| 1 | 0 | 2.72 | 1.36 |
| 1 | 1 | 5.44 | 2.72 |

**Table IV Maximum Output Frequency on CF**

| SCF | S1 | S0 | $F_{1-4}$ (Hz) | CF Max for AC Signals(Hz) |
|---|---|---|---|---|
| 1 | 0 | 0 | 1.7 | 128×F1,F2=43.52 |
| 0 | 0 | 0 | 1.7 | 64×F1,F2=21.76 |
| 1 | 0 | 1 | 3.4 | 64×F1,F2=43.52 |
| 0 | 0 | 1 | 3.4 | 32×F1,F2=21.76 |
| 1 | 1 | 0 | 6.8 | 32×F1,F2=43.52 |
| 0 | 1 | 0 | 6.8 | 16×F1,F2=21.76 |
| 1 | 1 | 1 | 13.6 | 16×F1,F2=43.52 |
| 0 | 1 | 1 | 13.6 | 8×F1,F2=21.76 |

## 12. Timing Characteristics

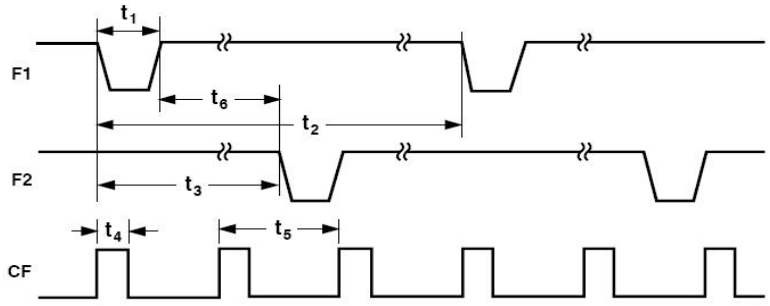
（VDD= 5V±5%, GND=0V, On-Chip Reference, CLKOSC=3.58MHz, $T_{MIN}$ to $T_{MAX}$ =-40～+85℃）

| Parameter | Specifications | Unit | Test Conditions/Comments |
|---|---|---|---|
| $T_1$ (1) | 275 | ms | F1 and F2 Pulsewidth (Logic Low) |
| $T_2$ | See Table III | s | Output Pulse Period, See Transfer Function Section |
| $T_3$ | 1/2 $T_2$ | s | Time between F1 Falling Edge and F2 Falling Edge |
| $T_4$ (1,2) | 90 | ms | CF Pulsewidth (Logic High) |
| $T_5$ | See Table IV | s | CF Output Pulse Period, See Transfer Function Section |
| $T_6$ | CLKOSC/4 | s | Minimum Time between F1 and F2 Pulse |

NOTES:

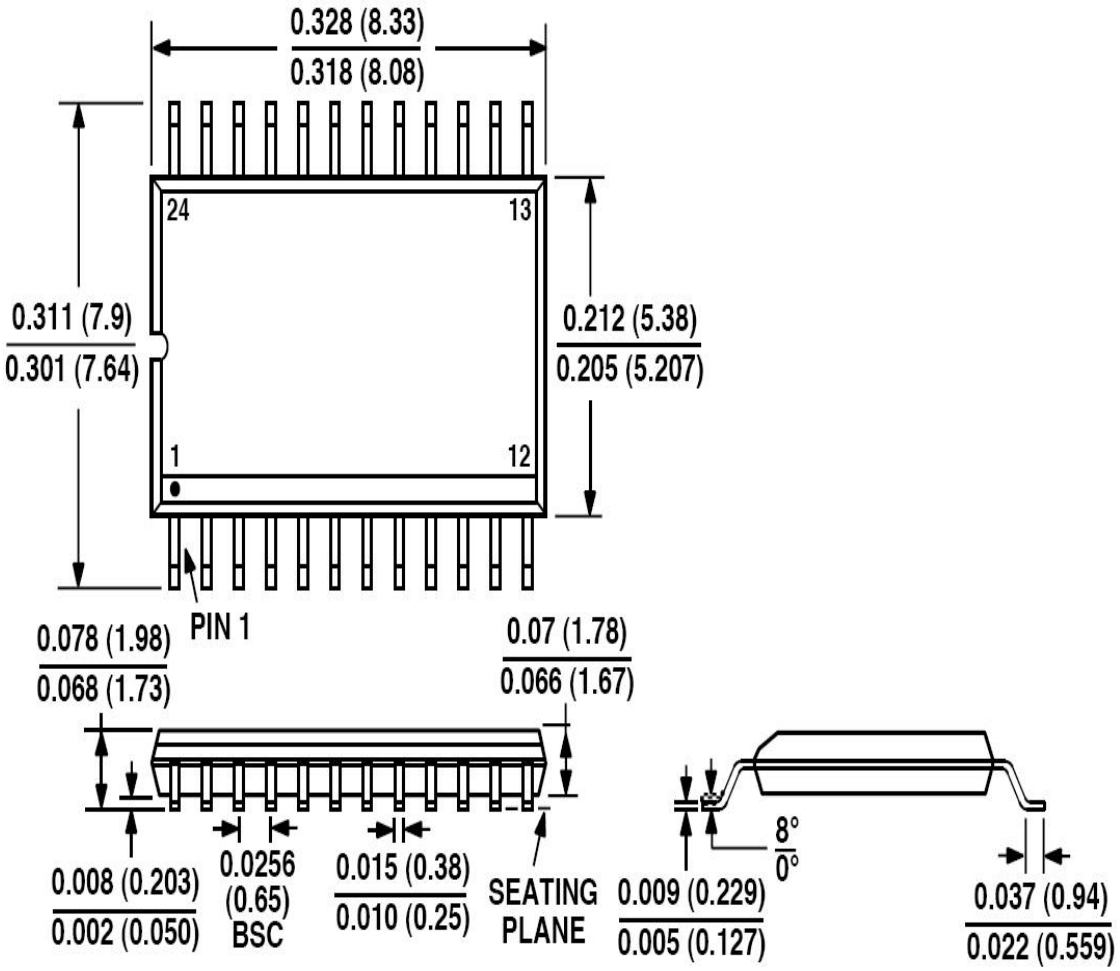
(1) The pulsewidths of F1, F2, and CF are not fixed for higher output frequencies.

(2) The CF pulse is always 18 µs in the high-frequency mode.




*Timing Diagram for Frequency Outputs*

## 13.Package Information (SSOP24)



## Special Instructions

The company reserves the right of final interpretation of this specification.

## Version Change Description

Version：V1.0 Author：Yang Time：2023.12.12

Modify the record：

1. Re-typesetting the manual and checking some data

Version：V1.1 Author：Chen Yang Time：2024.1.8

Modify the record：

1. Re-typesetting the manual and checking some data

# Statement

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