STT-MRAM Datasheet

PM002MNxB

Version:1.0

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Contents

1 Features

PM002 is a 2M Bit/256K Byte capacity SPI (Serial Single-Wire) interface STT-MRAM (Spin-Transfer Torque Magnetic Random Access Memory) chip. Its data is non-volatile with a retention time exceeding 10 years. The chip supports independent 1-bit SI (Serial Input) and SO (Serial Output) interfaces, allows continuous writing or reading of data bytes at its maximum clock frequency, and features zero write latency.

Density

- 2M Bit/256K Byte

Fast SPI interface with 8-bit data width addressing

- Up to 54MHz clock frequency @SPI SDR
- Support SPI Mode0 and SPI Mode3

Operation voltage

- Typical Voltage：3.3V

Data protection

- Protection mode with WP#EN, TBSEL, BP0, BP1, BP2 in mode register SR#1

Power consumption

- Sleep current 10μA (Typical value)
- Standby current 100μA (Typical value)
- Active current 12mA (Typical value @SPI 54MHz)

Package

- SOP8

Order specification

Part No	Density	Operating voltage range	Package	Devices per bag/reel	Maximum Program/Erase Cycles	Operating temperature	Data retention
PM002MNEB	2Mbit	2.7V~3.6V	SOP8	2500pcs/reel	1E10	-40℃~125℃	≥10years@105℃
PM002MNIB				2500pcs/reel		-40℃~85℃	≥10years@85℃

2 Pin Information

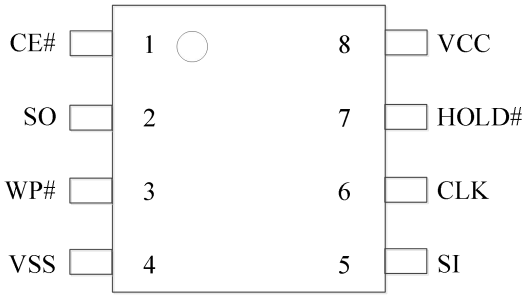


Figure 1: Package Information

3 Pin Description

Table1: Pin Description

No.	Symbol	Signal Type	Pin Description
1	CE#	Input	Chip Select Enable Signal
2	SO	Output	Serial Output
3	WP#	Input	Write Protect
4	VSS	Ground	Ground
5	SI	Input	Serial Input
6	CLK	Input	Serial Clock
7	HOLD#	Input	Hold
8	VCC	Power	Power

Pin Function Descriptions:

(1) CE#: Active-low chip select signal. The chip remains inactive (disabled) when CE# is de-asserted (high).

(2) SO: Data output pin, driven during data read operation, kept in high impedance state at other times, data output occurs at the falling edge of serial clock CLK.

(3) WP#: This is the pin for controlling the write operation to the SR register, which is used in conjunction with WP#EN. For details, please refer to Section 4.1.

(4) VSS: Ground.

(5) SI: All data are input to the chip through this pin and are sampled during the rising edge of the serial clock CLK. At other times, they are ignored.

(6) CLK: The clock input pin provides a clock signal for serial data input and output. The data on the SI pin is synchronized with the rising edge of CLK input, and the data on the SO pin is synchronized with the falling edge of CLK output. The chip supports SPI mode 0 (CPOL=0, CPHA=0) and SPI mode 3 (CPOL=1, CPHA=1). In mode 0, the clock is usually at a low level during idle time, and in mode 3, the clock is usually at a high level during idle time.

(7) HOLD#: When the pin remains at a low level, it will interrupt the current communication of the chip, making SO enter a high-impedance state, and CLK and SI become negligible. Keeping the pin pulled low is only allowed to occur when CE# is at a low level.

(8) VCC: Power.

4 SR Registers

The PM002 chip provides two SR registers, namely SR#1 and SR#2, which are stored in a volatile memory cell, and will be set to the initial value of 8'h0 0 after the chip is powered down and re-powered (but the value of the SR register is not lost after the chip enters sleep mode, After the chip exits sleep mode, the SR register remains at its previous value).

The bit allocation table of SR#1 and SR#2 is shown in Table 2.

Table 2: SR Register Bit Allocation Table

Registers	Data bit definition								Note
	7	6	5	4	3	2	1	0	
SR#1	WP#EN	RFU0	TBSEL	BP2	BP1	BP0	WREN	LOAD_BUSY	Part R，Part RW
SR#2	SRLK	RFU2	RFU1	DC4	DC3	DC2	DC1	DC0	RW

4.1 SR#1 Registers

In SR#1 register, WP#EN (Bit 7), TBSEL (Bit 5), BP2 (Bit 4), BP1 (Bit 3) and BP0 (Bit 2) are writable and readable; RFU0 (Bit 6), WREN (Bit 1) and LOAD_BUSY (Bit 0) are only readable. The default value of SR#1 register after power-on initialization of the chip is 8'h00.

After sending the write enable command, WREN (Bit1) becomes 1'b1; after sending the write disable command, WREN (Bit1) becomes 1'b0.

The main function of the SR#1 register is to define the write protection mode. When the chip is used as a part of non-volatile memory, the combination of TBSEL (Bit5), BP2 (Bit4), BP1 (Bit3), and BP0 (Bit2) defines the address range of the protected array area, and the remaining address range is the unprotected area; the combination of WP#EN (Bit7) and WREN (Bit1) defines how the write protection function is applied to the protected area, the unprotected area and the SR register. The protected state indicates that when the user writes other values to it, the write operation will fail; the unprotected state indicates that when the user writes other values to it, the write operation will succeed.

Table 3: Write protection features

WREN(SR#1)	WP#EN(SR#1)	WP#(Pin)	SR register	Protected Area	Unprotected Area
0	X	X	Protected status	Protected status	Protected status
1	0	X	Non-protected status	Protected status	Non-protected status
1	1	Low	Protected status	Protected status	Non-protected status
1	1	High	Non-protected status	Protected status	Non-protected status

Table 4: Protected area address ranges

TBSEL = 0			
BP2	**BP1**	**BP0**	**2Mb (4 blocks)**
0	0	0	No protected areas
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	1 block protected, address range(0x30000 – 0x3FFFF)
1	1	0	2 blocks protected, address range(0x20000 – 0x3FFFF)
1	1	1	3 blocks protected, address range(0x10000 – 0x3FFFF)
TBSEL = 1			
BP2	**BP1**	**BP0**	**2Mb (4 blocks)**
0	0	0	No protected areas
0	0	1	1 block protected, address range(0x00000 – 0xFFFF)
0	1	0	2 blocks protected, address range(0x00000 – 0x1FFFF)
0	1	1	3 blocks protected, address range(0x00000 – 0x2FFFF)
1	0	0	4 blocks protected, address range(0x00000 – 0x3FFFF)
1	0	1	
1	1	0	
1	1	1	

4.2 SR#2 Registers

In the SR#2 register, all bits are readable and writable. After the chip is powered on and initialized, the default value of the SR#2 register is 8'h00.

Note:

Although the RFU2 (Bit 6) and RFU1 (Bit 5) of SR#2 are reserved bits that can be read and written, for the chip to function properly, users must write 2'b00 to them.

The {DC4, DC0} (Bit4~Bit0) of SR#2 register defines the number of Dummy (idle clock cycles) between the end of the address input for the fast read operation and the first data output.

The SRLK of SR#2 defines the protection status of TBSEL (Bit 5) and BP2 to BP0 (Bits 4 to 2) of SR#1. When it is 1, TBSEL and BP2 to BP0 of SR#1 cannot be written and belong to the protected state. When it is 0, TBSEL and BP2 to BP0 of SR#1 can be written.

Table 5: Number and frequency of dummy for fast read operations

{DC4，DC0}	Dummy quantity	Frequency range of rapid reading operation(MHz)	Note
00h	0	0~40	Power-on default
01h	1	0~40	-
02h	2	0~40	-
03h	3	0~40	-
04h	4	0~40	-
05h	5	0~40	-
06h	6	0~40	-
07h	7	0~40	
08h~1Fh	8~31	0~54	-

5 Chip function

According to the SPI protocol, the first 8 bits of the input data are COMMAND (command code), which defines the operations that the chip will perform. Depending on the command code, there may follow 3-byte address, followed by idle clock cycles and data bytes, or directly followed by data bytes.

The 24-bit (3-byte) address part following some command codes defines the address that the chip will access. Given the current density of the storage array and the data bit width of 8 bits, the low 19 bits of the 24-bit address will be used as the valid address internally by the chip.

Note：

To prevent partial access to the chip, the user must keep CE# active within 8 times the clock period after CE# goes low.

The functions supported by the chip are shown in Table 6.

Table 6: Chip function chart

Command	SPI mode						
	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7~
Number of clocks	8	8	8	8	8 or configurable	8	8
SR#1 register write	01h	S7-S0					
SR#1 register read	05h	S7-S0					
SR#2register write	87h	S7-S0					
SR#2 register read	35h	S7-S0					
write	02h	A23-A16	A16-A8	A7-A0	D7-D0	D7-D0	D7-D0
Normal read	03h	A23-A16	A16-A8	A7-A0	D7-D0	D7-D0	D7-D0
Quick read	0Bh	A23-A16	A16-A8	A7-A0	Dummy (Quantity configurable)	D7-D0	D7-D0

Write enable	06h						
Write disable	04h						
Enter sleep mode	B9h						
Exit sleep mode	ABh						
Read Unique ID	4Bh	ID87~ID0					
Read MANU ID	9Fh	ID7~ID0					
Read Device ID	90h	ID7~ID0					
Reset enable	66h						
Reset	99h						

5.1 Control operations

The control commands include: write enable, write disable, enter sleep mode, and exit sleep mode.

The function of the write enable command is to allow the subsequent write commands, SR#1 register write commands and SR#2 register write commands sent by the user to take effect. The function of the write disable command is to prevent the subsequent write commands, SR#1 register write commands and SR#2 register write commands sent by the user from taking effect. The function of the enter sleep mode command is to make the chip enter sleep mode. The function of the exit sleep mode command is to make the chip exit sleep mode and enter standby mode.

The timing sequence of control commands is the same, only 8-bit command codes. For example, the timing sequence of the write enable command is shown in the following figure. The timing sequences of the enter sleep mode command and the exit sleep mode command are detailed in Chapter 7.

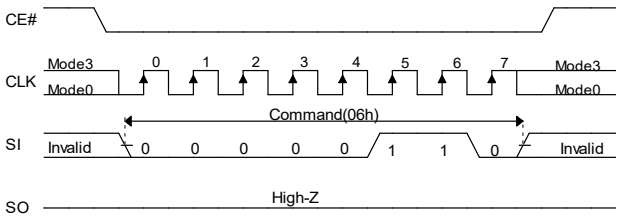


Figure 2: Writing Enable Command Timing Diagram

5.2 Reset operation

The reset operation requires the execution of two command codes: the reset enable command and the reset command. After the user executes these two commands in the prescribed sequence, the chip achieves the reset effect, and the values of all writable bits in the SR registers become the default value of 0. After a certain recovery time (tRST), the chip can perform normal read and write operations.

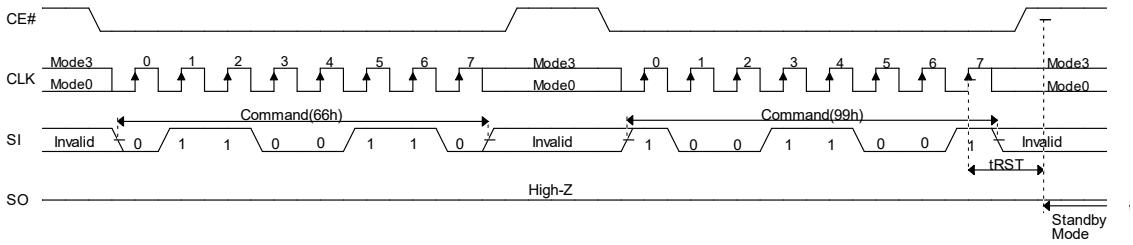


Figure 3: Reset Operation Timing Diagram

5.3 Write operation of SR register

The SR register write command allows writing new values to the SR#1 and SR#2 registers. The commands are 01h and 87h respectively. The timing sequence of the SR#1 register write command is illustrated in the following figure. The execution of the SR register write command requires first executing the write enable command, setting WREN to 1, and setting the values of WP# and WP#EN as shown in Table 3, so that the SR register is in a writable state.

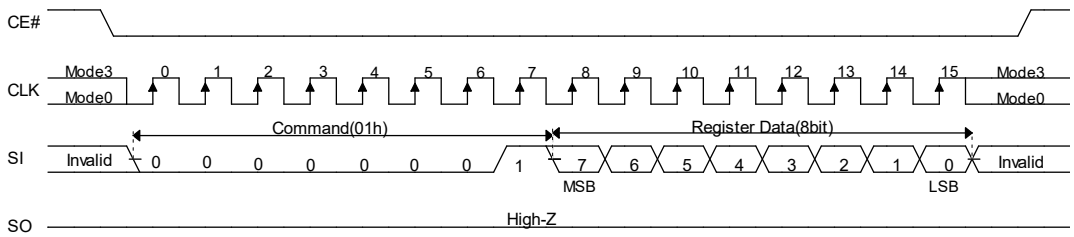


Figure 4: SR#1 Register Write Command Timing Diagram (Example)

5.4 Read operation of SR register

The SR register read command enables reading of SR#1 and SR#2 registers, with the commands being 05h and 35h respectively. The timing sequence of the SR#1 register read command is illustrated in the following figure.

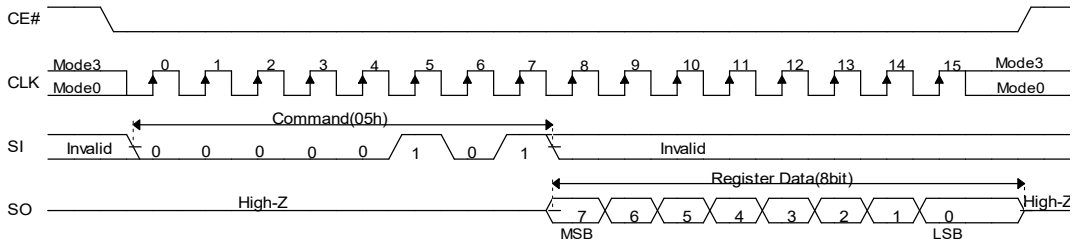


Figure 5: SR#1 Register Read Command Timing Diagram (Example)

5.5 Write operation

The write command allows writing data starting from the location specified by the 24-bit address. If CE# remains low continuously and CLK keeps flipping, the user can continue to send write data after the first data is sent. The chip will sequentially write the data to the subsequent addresses in order; when the address reaches the maximum address of the chip, the next address will roll over to the starting address 00h of the chip and repeat the process to write data to the entire chip indefinitely; until CE# is pulled high to terminate the write operation. Data written first within the same address will be overwritten by subsequent data written.

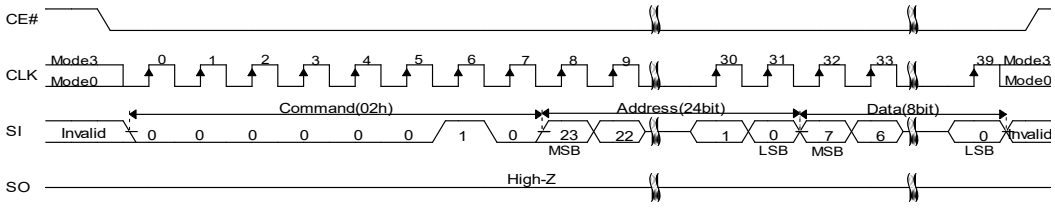


Figure 6: Writing Command Timing Diagram

5.6 Normal read operation

Normal read command allows data reading to start from the position specified by the 24-bit address. If CE# remains low continuously and CLK keeps flipping, the user can continue to receive read data after the first data reception is completed. The address will automatically increment, and the chip will successively read out the data in the subsequent addresses in sequence. When the address reaches the maximum address of the chip, the next address will roll over to the starting address 00h of the chip, and the entire chip's data will be read in an infinite loop; until CE# is pulled high to terminate the read operation.

Note:

1、 **The normal command reading function is only capable of handling frequencies no higher than 40 MHz.**

2、 **The normal reading of commands can only be executed when {DC4, DC0} of SR#2 register is set to 5'b00000. After the chip is powered on, {DC4, DC0} of SR#2 register is defaulted to 5'b00000.**

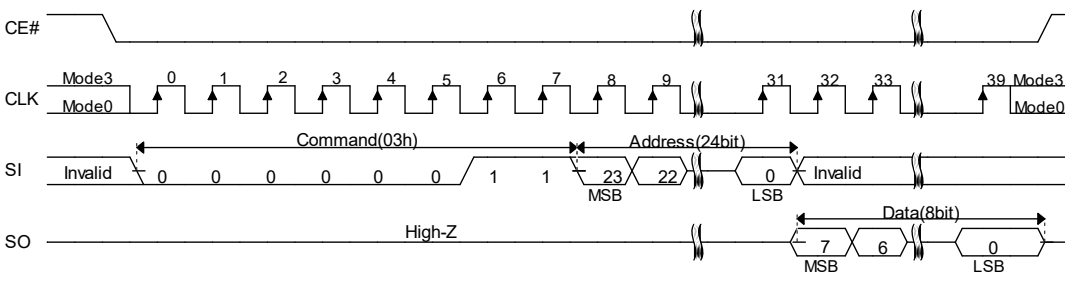


Figure 7: Normal Read Command Timing Diagram

5.7 Fast read operation

The quick read command enables data reading to start from the position specified by the 24-bit address. If CE# remains low continuously and CLK keeps flipping, the user can continuously receive the read data after the first data reception is completed. The address will automatically increment, and the chip will successively read out the data in the subsequent addresses in sequence. When the address reaches the maximum address of the chip, the next address will roll over to the starting address 00h of the chip, and the entire chip's data will be read in an infinite loop; the read operation will be terminated when CE# is pulled high.

The Quick Read command supports Dummy after the address is sent. The number of Dummies can be configured through the SR#2 register with {DC4, DC0}, ranging from 5'd0 to 5'd31. The default values of {DC4, DC0} on the chip are 5'd0 after power-on. The frequency range supported by the Quick Read command is related to the number of Dummies. For details, please refer to Section 5.2.

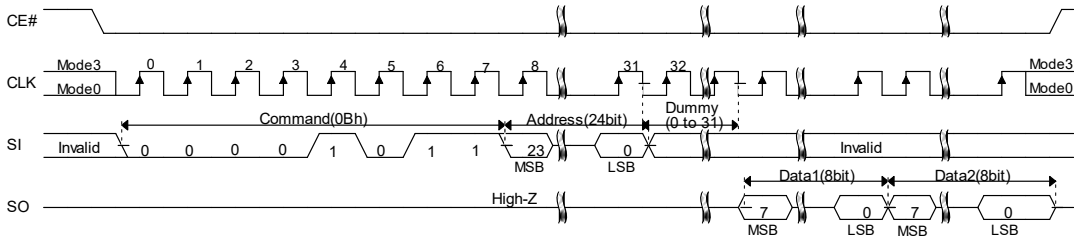


Figure 8: Fast Mode Read Command Timing Diagram

5.8 Read Unique ID Operation

The Unique ID of this chip is a total of 88 bits. It can be read via SPI command (4Bh). After sending out 8 bits of command code, the user can receive the Unique ID.

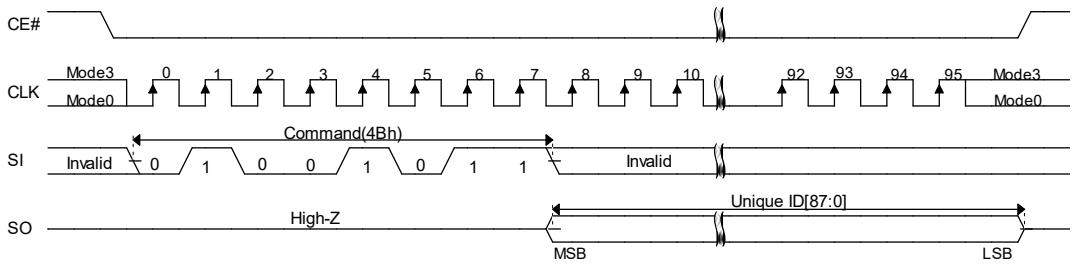


Figure 9: Reading Unique ID Command Diagram

5.9 Read Device ID Operation

The Device ID of this chip is 8 bits in total. It can be read via SPI command (90h). After sending out the 8-bit command code, the Device ID can be received by the user. The values of the Device ID are shown in Table 7, including product grade code and product capacity code.

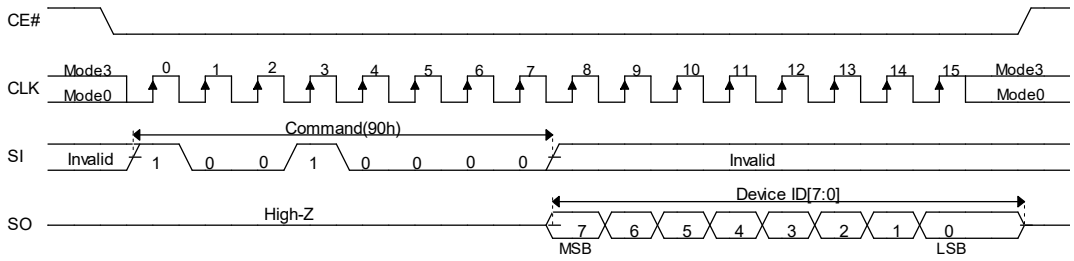


Figure 10: Reading Device ID Command Diagram

Table 7: Device ID Explanation

Device ID value	Device ID Explanation	
	7-5（3bit）	**4-0（5bit）**
	Product grade	**Product capacity**
29h	001	01001

5.10 Read MANU ID Operation

The MANU ID of this chip is 8 bits in total. It can be read via SPI command (9Fh). After sending out the 8-bit command code, the user can receive the MANU ID (26h).

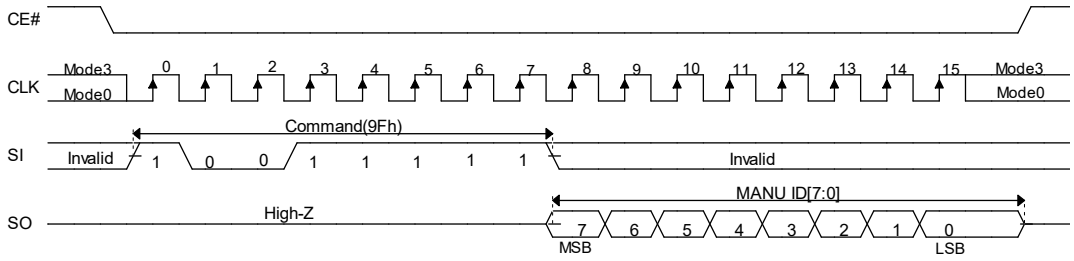


Figure 11: Reading MANU ID Command Diagram

6 Hold function

The HOLD# pin is used to sleep the serial communication of the chip and achieve the hold function. When the chip is selected and the serial communication is in progress, the HOLD# pin can sleep the serial communication between the chip and the user, and the user does not need to reset the ongoing serial sequence. When the user needs to sleep the communication, simply pull down the HOLD# pin when the CLK pin is at a low or high level; when the user needs to resume the communication, simply pull up the HOLD# pin when the CLK pin is at a low or high level. During the period when HOLD# is at a low level, the CLK pin can flip. When the communication between the chip and the user is sleeped, the input value on the SI pin will be ignored, and the SO pin is in the High-Z state.

It should be noted that if the HOLD# pin is pulled low during the period when the CLK pin is at a low

level, then the HOLD# pin needs to be returned to a high level during the same period; if the HOLD# pin is pulled low during the period when the CLK pin is at a high level, then the HOLD# pin needs to be returned to a high level during the same period.

If during the period when HOLD# is at a low level, CE# is pulled high, the current operation will be terminated; if before HOLD# is pulled low, the 8-bit command code has not been sent completely, then during the period when HOLD# is at a low level, CE# is pulled high, the current command will have no effect at all.

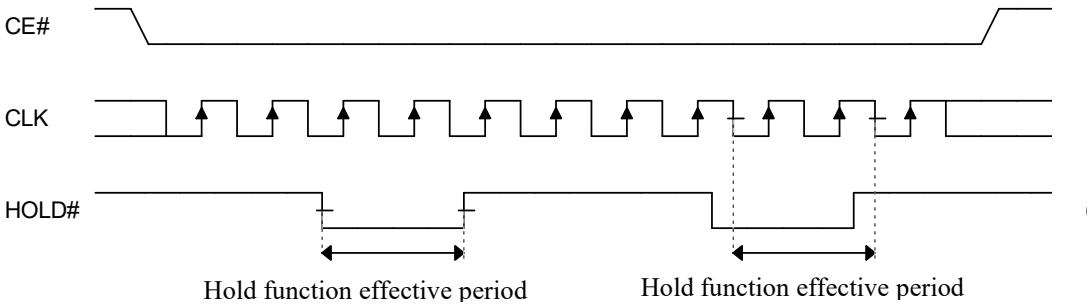


Figure 12: Hold Mode Functional Sequence Diagram

7 Chip mode

This chip offers three modes: working, standby, and sleep. In the working mode, there are mainly read operations and write operations.

After power-on, when the chip initialization process is completed, the chip enters the standby mode. The chip cannot receive command codes, and the data in SI is invalid, while SO remains in the High-Z state. Then, when the user pulls down CE# and the sent command code is not B9h, the chip enters the operation mode and can receive the address and data on SI and read or write the data at the specified address according to the command code; when the user pulls down CE# and the sent command code is B9h, the chip will enter the sleep mode. In this case, the internal power supply of the chip will be turned off, and no read or write operations can be performed. In the operation mode, when the user pulls up CE#, the chip returns to the standby mode. In the sleep mode, when the user pulls down CE# and issues the command to exit the sleep mode (i.e., ABh), the chip will perform the wake-up operation, re-enable the internal power supply, and switch from sleep mode to standby mode.

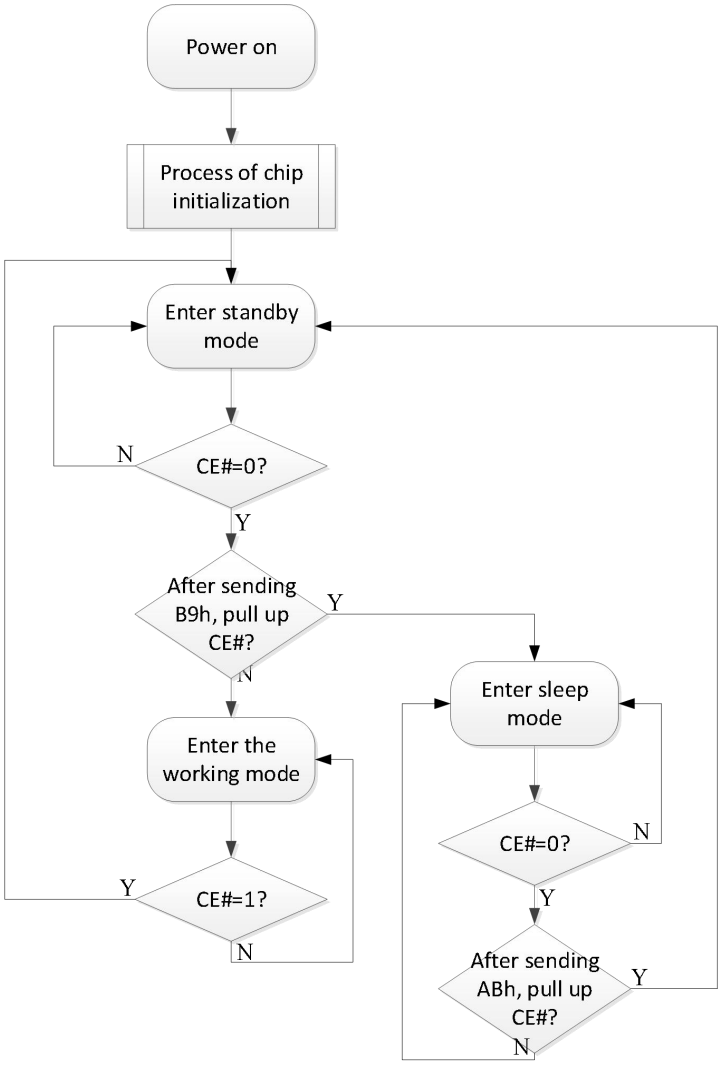


Figure 13: Chip Mode Switching

7.1 Enter sleep mode

Sleep mode is a low-power mode. Once the chip enters this mode, the internal power supply is turned off to save power consumption. Users can issue a command to enter the sleep mode (B9h), and after a certain period of time (tESLP), the chip will enter this mode.

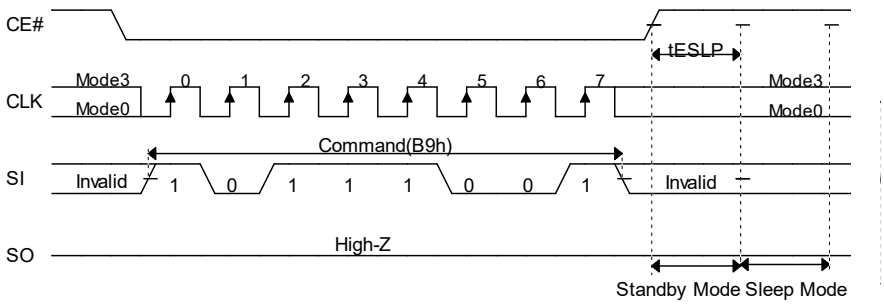


Figure 14: Entering Sleep Mode Timing Diagram

7.2 Exit sleep mode

When the chip is in the sleep mode, the user can issue the command (ABh) to exit the sleep mode and make the chip enter the wake-up process. During the wake-up process, the internal power supply module will be re-enabled. After the wake-up process is completed, the chip enters the standby mode. The time required for the wake-up process is t_{RSLP}.

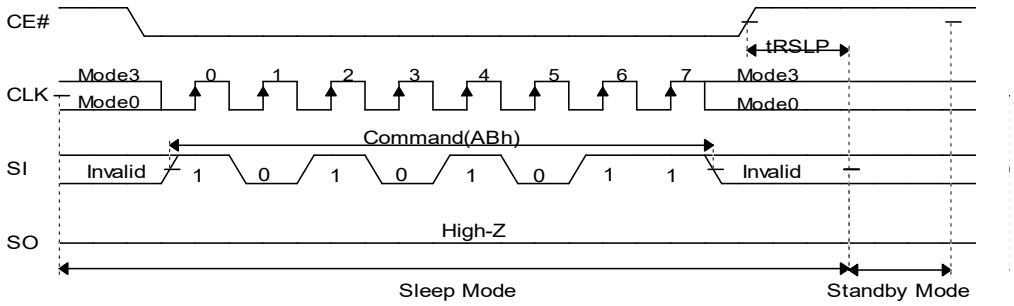


Figure 15: Exiting Sleep Mode Timing Diagram

8 Input/Output Interface Timing Sequence

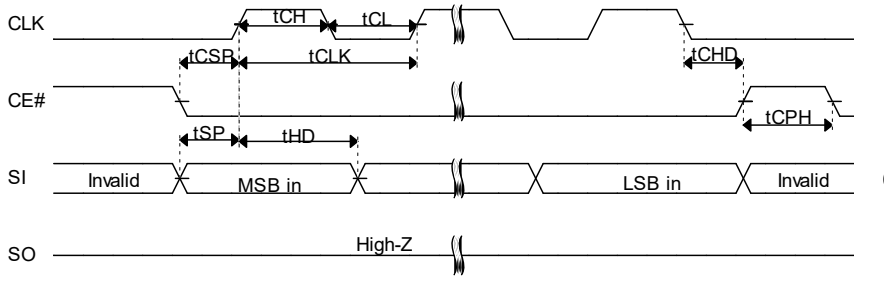


Figure 16: Input Interface Timing Diagram

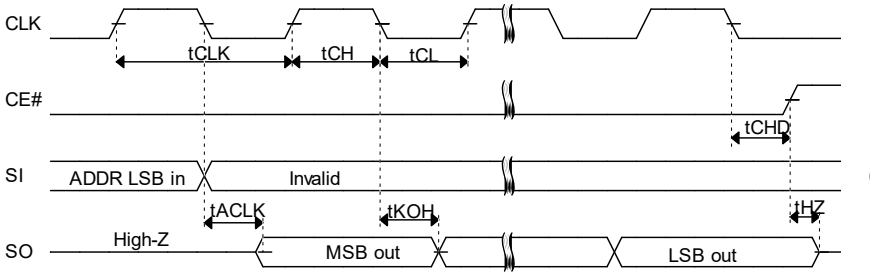


Figure 17: Output Interface Timing Diagram

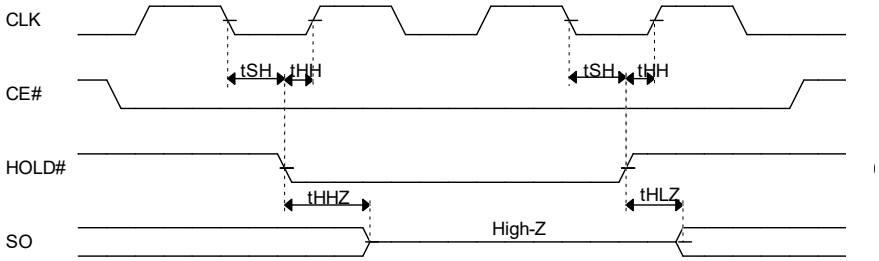


Figure 18: HOLD# Interface Timing Diagram 1

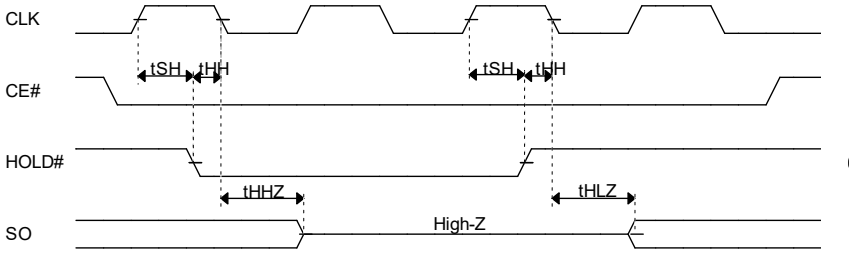


Figure 19: HOLD# Interface Timing Diagram 2

9 Absolute Maximum Rating

Table 8: Absolute Maximum Rating

Symbol	Parameter	Test Conditions	Value	Unit
VCC	Power supply voltage		-0.5~4	V
V_{IN}	Any pin voltage		-0.5~(VCC+0.5)	V
I_{OUT}	Each pin output current		±20	mA
T_{BIAS}	Temperature under bias pressure	Industrial grade	-40~125	℃
T_{stg}	Storage temperature		-55~150	℃
H_{max_write}	Maximum magnetic field	Write	4,000	A/m

	during writing			
H_{max_read}	Maximum magnetic field during reading or standby mode	Reading or standby	12,000	A/m
$H_{max\_poweroff}$	Maximum magnetic field during power off	Power off	40,000	A/m

10 AC/DC characteristics

This chapter introduces the AC/DC characteristics of the chip. The AC and DC parameter values shown in the table are derived from the tests conducted under the working conditions indicated in Table 9 and the measurement conditions noted in Tables 10 and 12. When users refer to a certain parameter, the working conditions and measurement conditions should be consistent.

10.1 Operating conditions

Table 9: Operating conditions

Symbol	Parameter	Min	Max	Unit
VCC	Power supply voltage	2.7	3.6	V
T_A	Temperature (industrial)	-40	125	℃

10.2 DC characteristics

Table 10: DC Characteristics

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$\|I_{LI}\|$	Input leakage current	0≤ CE# ＜VCC	-	-	140	μA
		CE# = VCC	-	-	1	μA
		WP#, HOLD#, CLK, SI = 0V~VCC	-	-	1	μA
$\|I_{LO}\|$	Output leakage current	SO = 0V~VCC	-	-	1	μA

I_{SLP}	Sleep current	CE# = VCC All inputs VSS or VCC		-	10	145	μA
I_{SBY}	Standby current	CLK = SI = CE# = VCC		-	100	5600	μA
I_{CC}	Operating current	SPI Write	CLK = 1MHz	-	9	16	mA
			CLK = 40MHz	-	11	18	mA
			CLK = 54MHz	-	12	19	mA
		SPI Read	CLK = 1MHz	-	5	13	mA
			CLK = 40MHz	-	7	15	mA
			CLK = 54MHz	-	8	16	mA
V_{IL}	Input low level	VCC = 2.7V~3.6V		-0.3	-	0.8	V
V_{IH}	Input high level	VCC = 2.7V~3.6V		VCC-0.4	-	VCC+0.3	V
V_{OL}	Output low level	I_{OL} = 3.1mA		-	-	0.2VCC	V
V_{OH}	Output high level	I_{OH} = -3.1mA		0.8VCC	-	-	V

10.3 Pin capacitance

Table 11: Pin Capacitors

Symbol	Parameter	Typ.	Max	Unit
C_P	External capacitors for VCC/VSS power supply	-	10	μF
C_{IN}	Control input capacitor	-	8	pF
C_{IO}	IO capacitor	-	12	pF
C_{LOAD}	Load capacitance	-	32	pF

10.4 AC characteristics

Table 12: Test Conditions for AC Characteristics

Parameter	Value	Unit
Power supply voltage range	2.7~3.6	V
Temperature range (industrial)	-40~125	℃
Input interface voltage range	VCC - 0.4 ≤ V_{IH} ≤ VCC + 0.3 0 ≤ V_{IL} ≤ 0.8	V
Rising edge time of input interface	2	ns
Descending edge time of input interface	2	ns
Input interface judge the level of the adopted voltage value	VCC/2	V
Input interface judge the level of the adopted voltage value	VCC/2	V

Table 13: AC Characteristics

Symbol	Parameter	Min	Max	Unit
f_{CLK}	CLK Clock frequency	0	54	MHz
t_{CH}/t_{CL}	Clock high/low level time	9	-	ns
t_{CPH}	Minimum high-level time between each instruction switch of CE#	150	-	ns
t_{CSP}	Setup time of CE# at the rising edge of the clock	10	-	ns
t_{CHD}	CE# hold time starting from the rising edge of the clock	10	-	ns
t_{SP}	Input data setup time on the rising edge of the clock	2	-	ns
t_{HD}	Input data hold time from the rising edge of the clock	5	-	ns
t_{HZ}	The switching time when the output data becomes invalid	3	6	ns

t_{ACLK}	Output data becomes valid switching time	-	9	ns
t_{KOH}	Output data hold time	4	-	ns
t_{RST}	Reset recovery (normal reading and writing) time	500	-	μs
t_{ESLP}	Time from entering sleep mode command to entering sleep mode	-	10	μs
t_{RSLP}	Time from exiting sleep mode to entering standby mode	500	-	us
t_{SH}	HOLD# setup time	10	-	ns
t_{HH}	HOLD# hold time	10	-	ns
t_{HHZ}	HOLD# is pulled low to output Hi-Z time	-	20	ns
t_{HLZ}	HOLD# pulled high to output valid time	-	20	ns

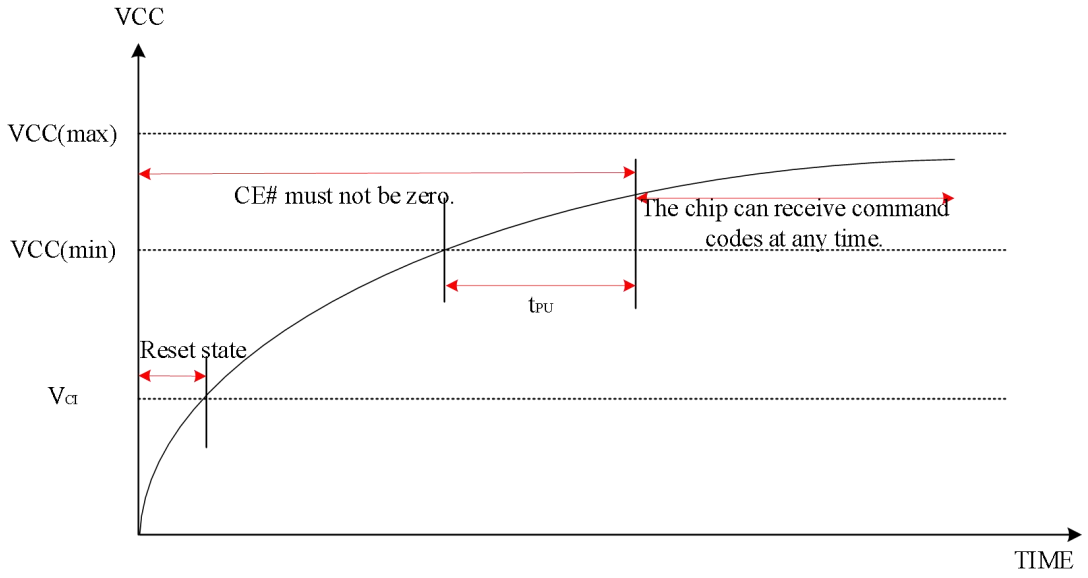
10.5 Power-up characteristics

To provide protection for data during the initial power-on and power-off re-ON periods, whenever VCC is lower than the specified minimum voltage (VCC(min)), the chip cannot be selected (CE# is internally limited to a high level within the chip), and the chip cannot complete read or write operations.

During the initial power-on or during the power-up after a power-off, the chip can start to work normally only after the voltage has risen to the specified minimum voltage (VCC(min)) for the time required beyond the power-on delay time (t_{PU}). This time is used to ensure that the internal voltage of the chip has stabilized. t_{PU} is measured from the moment when the voltage reaches the specified minimum voltage (VCC(min)).

Table 14: Power-on Initial Voltage and Delay Time

Symbol	Parameter	Min	Max	Unit
V_{CI}	Power on Initial voltage	2.35	-	V
t_{PU}	Power on delay time	500	-	μs



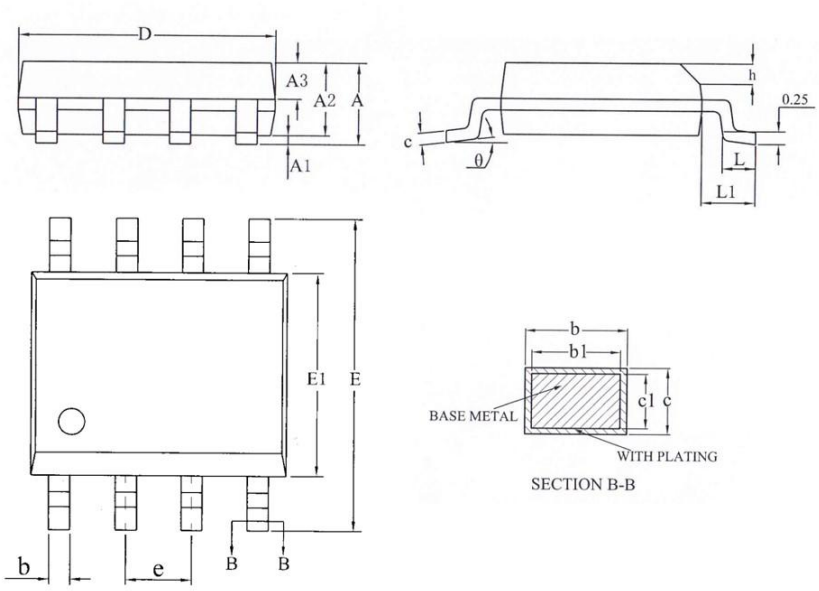
Note:
VCC(min) refers to the minimum value of VCC stipulated for normal operation of the chip, which is 2.7V in this chip;
VCC(max) refers to the maximum value of VCC stipulated for normal operation of the chip.

Figure 20: Diagram of Power-on Process

11 Note of Use

We suggest that users program the chips after reflow soldering. Since we cannot guarantee that the data written before reflow soldering will remain valid after the process, we recommend doing the programming after the reflow soldering.

12 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 21: SOP8 Package Shape

Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version：V1.0	Author：Zhao	Time：2025.03

Modify the record：

1. Editio princeps

Statement

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