32-bit powerline carrier-specific MCU based on CORTEX M4, 150 MHz, 512KB FLASH, 256KB RAM 3xUART, SPI, IIC, Timers, ADC

Directory

1. Version history

Version history	Version modification description
First edition	2024-08-01

2. Overall overview

2.1 Introduction to the chip

This chip is a highly integrated SOC chip that supports HPLC communication, and the physical layer meets the State Grid Q/GDW12087.41 standard. Using advanced digital-analog hybrid design technology , HPLC analog front-end circuits, digital signal processing circuits, memory and MCUs are completely implemented on a single chip, thereby completing the modulation and demodulation of data and protocol layer processing.

The HPLC communication channel of this chip adopts OFDM modulation and demodulation, supports signal frequency range 200KHz to 12MHz, can support up to 411 subcarriers, subcarriers support BPSK, QPSK and 16QAM mapping to achieve different rate modes, and the physical layer can reach up to 12Mbps transmission speed. The chip has built-in powerful Turbo forward error correction and interweaving technology, and the transmission mode can be flexibly configured, so that it can achieve reliable communication even under extremely strong noise interference.

The chip integrates a 32-bit MCU core and rich on-chip resources to meet the software functions and application development needs of the MAC layer and above protocol layer of power grid dual-mode communication.

The operating temperature range of this chip is -40°C~+85°C.

2.2 Chip block diagram

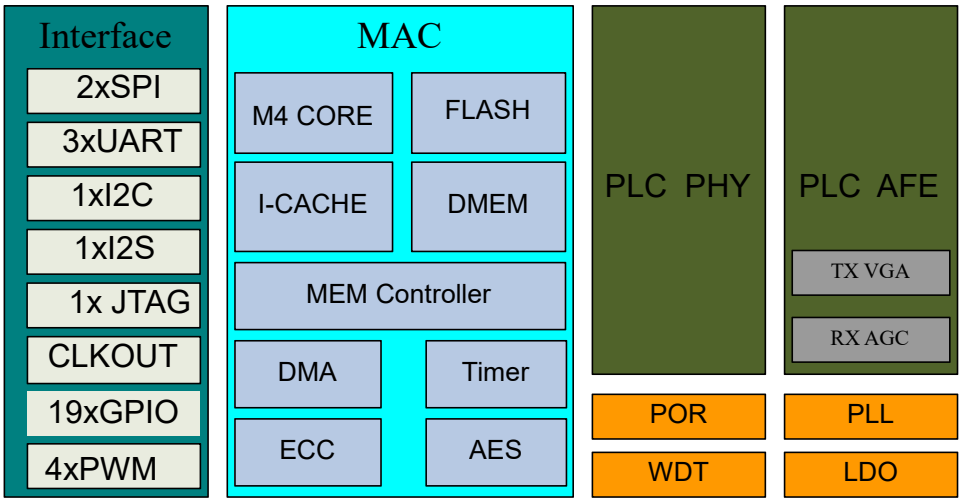


Figure 2.1: System structure block diagram

2.3 Basic characteristics

- Core: Arm 32-bit Cortex-M4, maximum frequency 150MHz
- -40 to 85°C operating temperature
- Memory
  —512K FLASH
  —256K SRAM
- CRC cycle calibration unit
- Reset and power management unit
  —Working voltage: 1.2V, 3.0~3.6V
  —POR/PDR
- Communication interface
  —3 UART

—2 SPI
—2 IIC

- Clock management unit
  — Master clock: 25M
  — Internal 32K
- GPIO
  — 19 GPIOs
  — 4 PWM outputs
- ADC
  — 4 ADC channels
- 5 timers with input capture
- Support 4-wire JTAG debugging mode
- 150KHz-12MHz carrier

2.4 Scope of application

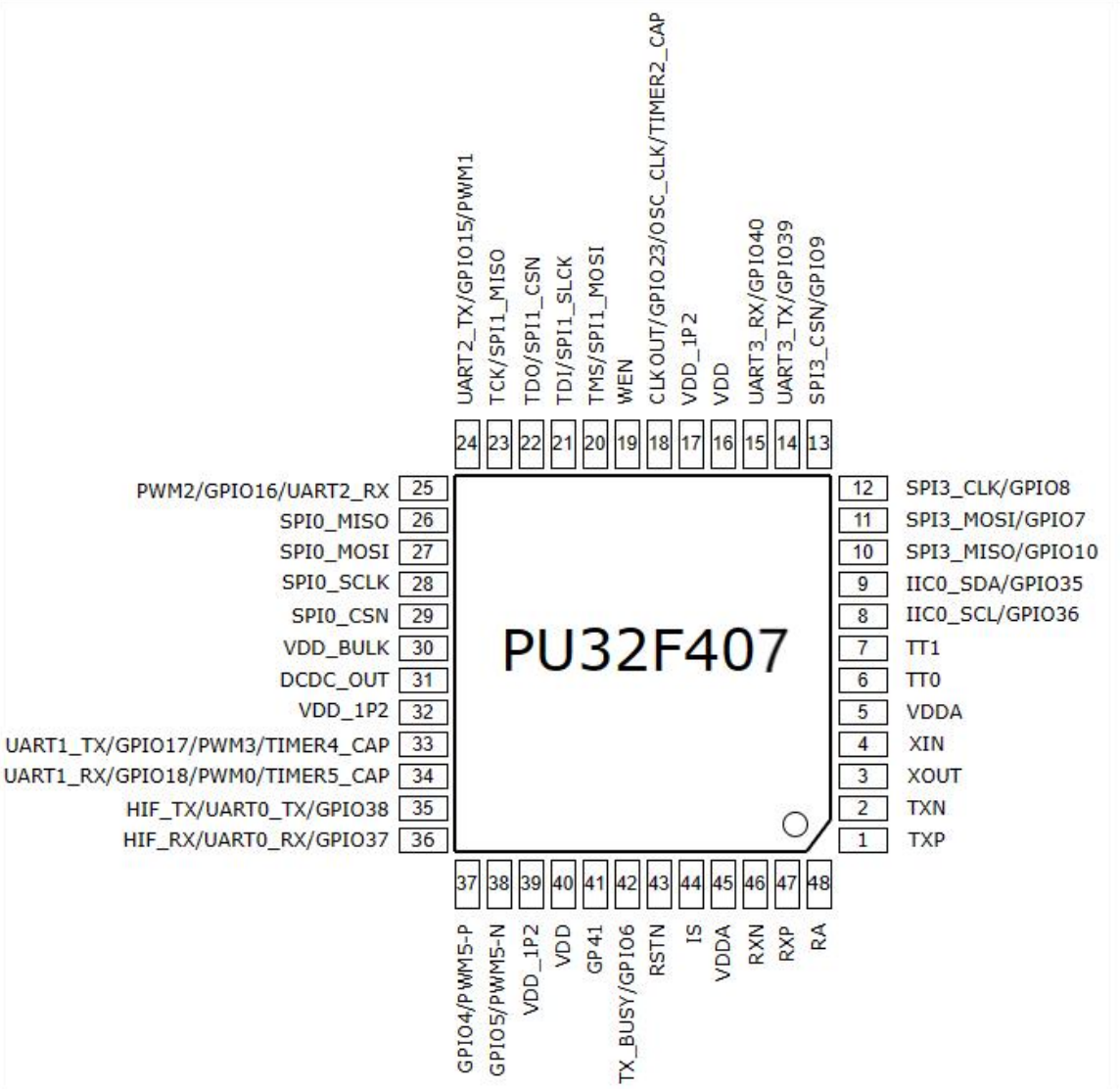
- Remote automatic meter reading
- Internet of Things and Smart Home
- Lighting control
- Industrial control automation
- Smart building control
- Photovoltaic control

2.5 Abbreviations

Abbreviations	illustrate
ADC	Analogue to Digital Converter
AGC	Automatic Gain Control
AMP	Amplifier
AMR	Automatic Meter Reading
ARQ	Automatic Repeat Request
BOR	Brown Out Reset
BPF	Band Pass Filter
CRC	Cyclic Redundancy Check
DAC	Digital to Analogue Converter
DDS	Direct Digital Converter
FFT	Fast Fourier Transformation
GPIO	General Purpose IO
HIF	Host Interface
IRQ	Interrupt Request
ISI	Inter Symbol Interference
LDO	Low Drop Out linear regulator
LVD	Low Voltage Detect
OFDM	Orthogonal Frequency Division Multiplexing
OSC	Oscillator
PDM	Pluse Density Modulation

PGA	Programmable Gain Amplifier
PLC	Power line communication
POR	Power On Reset
PPDU	PHY Packet Data Unit
PS0	Program memory Section0
PS1	Program memory Section1
PSM	Power Saving Mode
RTC	Real Time Clock
RSSI	Received Signal Strength Indication
SCM	System Clock Management
SFR	Special Function Register
SPI	Serial Peripheral Interface
UAM	User Application Mode
VGA	Voltage Gontral Amplifier
WDT	Watch Dog Timer

2.6 Pin distribution



2.7 Pin Instructions

Pins	Symbol	Type	Function description
1	TXP	A	The output pin of the chip DAC has an output amplitude of 0-2Vpp
2	TXN	A	The output pin of the chip DAC has an output amplitude of 0-2Vpp
3	XOUT	A	Crystal clock output
4	XIN	A	Crystal clock input
5	VDDA		Analog power supply, 3.3V input, plus 0.1uF capacitor
6	TT0	IO	Test the relevant pins, connect GND
7	TT1	IO	Test the relevant pins, connect GND
16	VDD		Digital power supply, 3.3V input, plus 0.1uF capacitor

17	VDD1P2		The digital core is 1.2V, with a 0.1uF decoupling capacitor added. All the 1.2V components need to be connected together externally
30	VDD_BUCK		BUCK power supply 3.3V input with 4.7uF and 0.1uF capacitors
31	DCDC		BUCK PWM signal output signal, the recommended value of off-chip inductance is 10uH, and the recommended value of off-chip capacitance is 10uF
32	VDD1P2		Connect the BUCK output 1.2V, external 0.1uF capacitor, all 1.2V need to be connected externally
39	VDD1P2		The digital core is 1.2V, plus 0.1uF decoupling capacitor, and all 1.2V needs to be connected externally
40	VDD		Digital power supply, 3.3V input, plus 0.1uF capacitor
43	RSTN	I	Reset pin, 10K pull-up inside the chip, effective at low level, reset time > 5ms
44	IS	A	The input pin bias current is set pin, and the external resistor is connected to 30kΩ 1% resistor to ground
45	VDDA		Analog power supply, 3.3V input, plus 0.1uF capacitor
46	RXN	A	The differential signal is input to the negative end
47	RXP	A	The differential signal is input at the positive end
48	RA	A	Test pin, floating

2.8 Analog related pin description

2.9 Digital Pin and Multiplexing Chart

Number	Name	Default features	Fuction 0	Fuction 1	Fuction 2	Fuction 3
8	GPIO36	GPIO	MCU SCL0			
9	GPIO35	GPIO	MCU SDA0			
10	GPIO10	GPIO	SPI3 MISO	GPIO	DC_IN_3	
11	GPIO7	GPIO	SPI3 MOSI	GPIO	DC_IN_4	
12	GPIO8	GPIO	SPI3 SCLK	GPIO	DC_IN_1	
13	GPIO9	GPIO	SPI3 CS_N	GPIO	DC_IN_2	
14	GPIO39	GPIO	UART3_TX			
15	GPIO40	GPIO	UART3_RX			
18	GPIO23	GPIO	MAC CLK	OSC CLK	Timer2 capture	I2S_MCLK
19	WEN	Function 0	Watchdog EN	GPIO		
20	JTAG_TMS	Function 0	MCU TMS(default)	SPI1 MOSI(Default master)	GPIO	I2S_DI
21	JTAG_TDI	Function 0	MCU TDI(default)	SPI1 SCLK(Default master)	GPIO	I2S_BCLK

22	JTAG_TDO	Function 0	MCU TDO(default)	SPI1 CS_N(Default master)	Timer3 capture	I2S_LRCLK
23	JTAG_TCK	Function 0	MCU TCK(default)	SPI1 MISO(Default master)	GPIO	I2S_DO
24	GPIO15	GPIO	UART2_TX	GPIO	PWM1	
25	GPIO16	GPIO	UART2_RX	GPIO	PWM2	
26	SPI0_MOSI	Function 0	SPI0			
27	SPI0_MOSI	Function 0	SPI0			
28	SPI0_SCLK	Function 0	SPI0			
29	SPI0_CSN	Function 0	SPI0			
33	GPIO17	GPIO	UART1_TX	GPIO	PWM3	Timer4 capture
34	GPIO18	GPIO	UART1_RX	GPIO	Timer5 capture	PWM0
35	GPIO38	GPIO		UART0 TX		
36	GPIO37	GPIO		UART0 RX		
37	GPIO4	GPIO				
38	GPIO5	GPIO	Timer0 capture	I2S1_MCLK		
41	GPIO41	GPIO				
42	GPIO6	GPIO	TX_BUSY			

2.10 Absolute Maximum Ratings

ITEM	RANGE	UINTS
VDD to GND	-0.5～+4.0	V
IO to GND	-0.5～+4.0*	V
Continuous Power Dissipation	1500(derate 25mW/℃,above 70℃)	mW
Operating Temperature Range	-40～+85	℃
Storage Temperature Range	-50～+150	℃
Lead Temperature(soldering,10S)	300	℃

Note:

1. Some IOs with open leakage function support 5.5V withstand voltage, and using the chip beyond the limit parameters may lead to permanent failure of the chip.

2.11 Electrical characteristics

2.11.1 Electrical specifications of CMU module

To be added

2.11.2 Electrical specifications of PMU module

To be added

2.12 Package size

2.12.1 Marking instructions

Figure 2.5: Marking instructions

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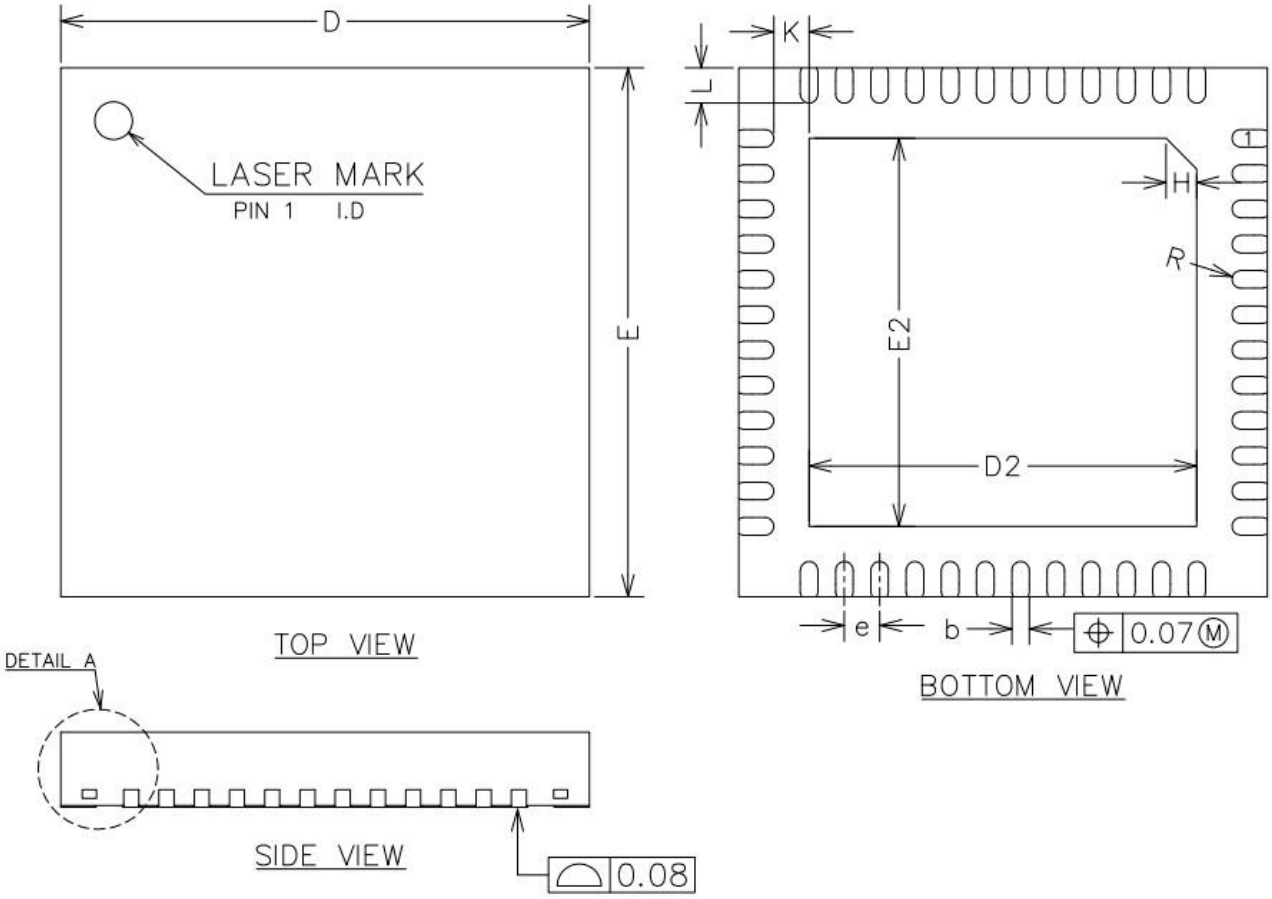
- The 1st~3rd digit (xxx) is the product batch number
- A means assembly factory
- The last 3 digits (xxx) are DATE CODE

2.12.2 QFN48 package size



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	4.30	4.40	4.50
E2	4.30	4.40	4.50
e	0.30	0.40	0.50
H		0.35REF	
K	0.30	0.40	0.50
L	0.30	0.40	0.50
R	0.075	–	–

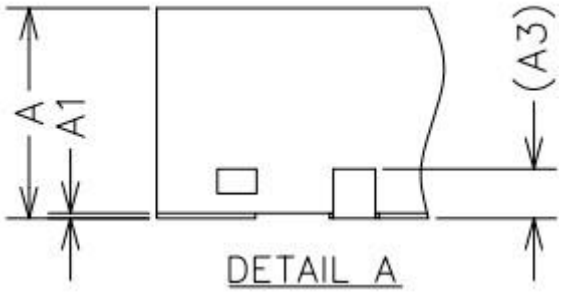


Figure 2.8: QFN48-6X6 package size

2.13 Packaging specifications

Model	Packing method	Quantity per tray
PU32F407	tray	490PCS/tray (35x14).

3. AES module

3.1 Overview

The AES algorithm is a symmetric encryption and decryption algorithm that uses the same key for encryption and decryption.

Key lengths are 128-bit, 192-bit, and 256-bit.

The input data is grouped by 128-bit length, and if the length of the input data is not an integer multiple of 128-bit, it needs to be filled.

The output data length is equal to the input data length.

3.2 List of functions

- Key length is configurable
  - 128bit
  - 192bit
  - 256bit
- Algorithm mode configurable
  - ECB mode
  - CBC mode
- Supports encryption or decryption
- Supports GCM mode
- Supports starting finite domain multiplication units separately
- Data size is configurable
- Support automatic key expansion: keys of different lengths will be generated internally through key expansion
- Use one DMA channel to enter plaintext data and another DMA channel to output ciphertext data
- Encryption and decryption are supported to complete interruptions

4. CMU module

4.1 Overview

The chip supports the following system clock sources

- 25MHz clock provided by an external crystal oscillator.
- An external crystal oscillator provides a 25MHz clock, which is multiplied on-chip to obtain PLL clocks of 200MHz, 250MHz, and 300MHz..
- An external crystal oscillator provides a 25MHz clock, which is then divided on-chip to obtain a 32.768kHz clock.

4.2 Clock block diagram

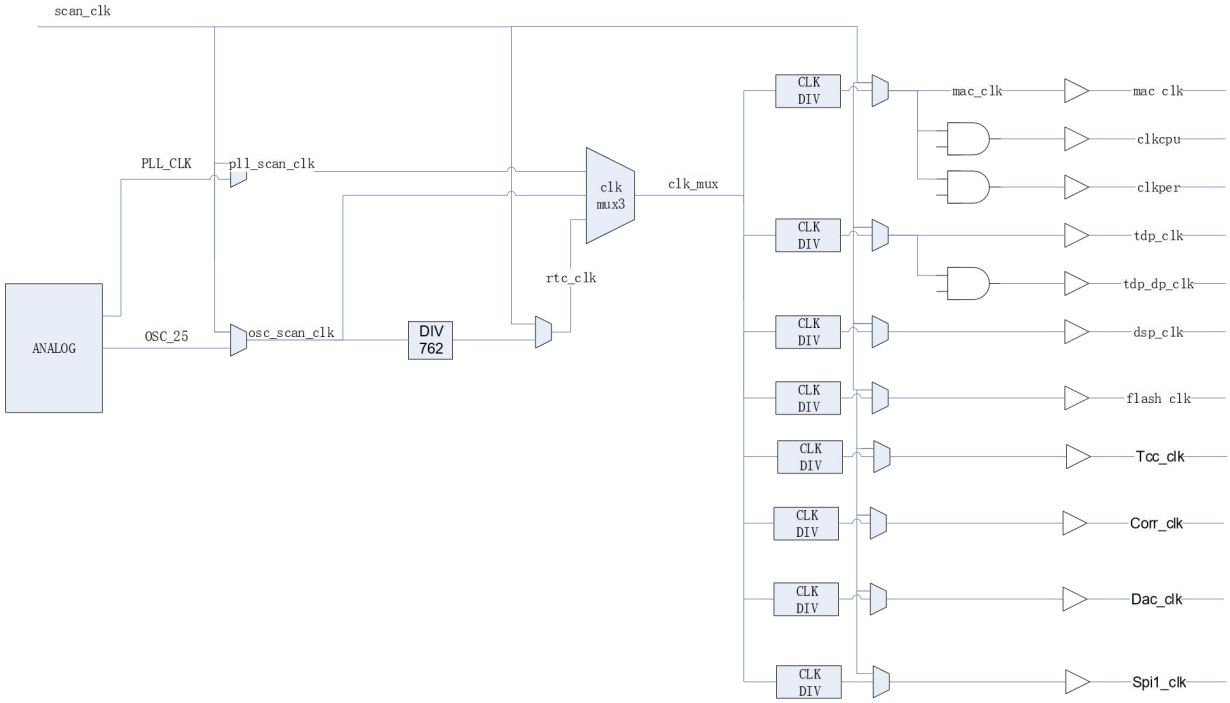


Figure 4.1: Clock block diagram

The clock is described as follows:

- Flf: The internal division low-frequency clock, which is divided by the reference clock source Fhse.
- FHSE: External high-frequency HSE clock.
- Fpll: Internal high-frequency PLL clock (3 gears adjustable), reference clock source is Fhse.

4.3 Clock description

4.3.1 Internal division frequency low frequency clock

The internal frequency division low-frequency clock (Flf) is divided by an external crystal oscillator and has a frequency of 32.768KHz.

4.3.2 External high-frequency HSE clock

The external high-frequency HSE clock (Fhse) is provided by a 25MHz crystal, and the crystal reference circuit is shown below.

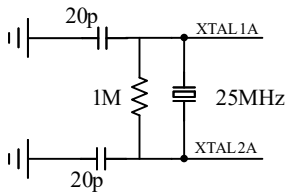


Figure 4.2: Crystal peripheral circuit diagram

4.3.3 Internal High Frequency PLL Clock

The internal high-frequency PLL clock (Fpll) is obtained by the 25MHz clock doubling provided by an external crystal oscillator (HSE).The HSE clock is upscaled by 8x, 10x, or 12x, and the PLL outputs a 200MHz, 250MHz, or 300MHz clock to the MCU and PHY system.

There is a PLL clock lock detection module inside the chip, and the clock lock flag will be reflected on the register PllStatus.bit[2], which can be queried by the user to determine whether the PLL has entered the locked state. If the bit is 1, the PLL is locked and the user can switch the system clock to the PLL clock.

Note:

1. The PLL's master switch must be turned on before the PLL clock can be enabled.
2. The total switch of the PLL is controlled by bit0 and bit1 of the register HPLCPhyEnCtl.

4.3.4 Clock source selection and clock frequency division

The chip has 3 selectable system clock sources, including Fhse, Fpll, and Flf clocks. The clock source selection module is responsible for selecting one of the clock sources as the working clock. The clock divider module has multiple sets of clock dividers, which can be divided by the working clock source and provided to the various functional modules of the MAC subsystem.

Functional modules	Enter the clock source	Maximum	Minimum	Description
System clock	PLL/HEE/LF	300M	32K	The clock source selection module is responsible for selecting from Fpll (200/250/300MHz), Fhse (25MHz) or Flf (32.768KHz) is selected as the working clock source. The working clock source serves as the distributor source of the clock of each function module.
MAC sub-clock	NO	200M	32K	The MAC clock must always be on. The frequency of the MAC clock can be adjusted via the configuration register MacClkDiv.
FLASH controller clock	NO	50M	32K	Access the off-chip Flash serial clock with a clock source of Fhse or Fpll/1.5. The clock frequency can be adjusted through the QSPI module.

4.4 Electrical specifications of CMU module

4.4.1 Clock source vibration time

(To be added)

4.4.2 Clock source power consumption

(To be added)

5. CRC module

5.1 Overview

CRC or Cyclic Redundancy Check, is the most commonly used error checksum in the field of data communication, which performs polynomial calculations on the data and attaches the results to the data frame. The receiving device performs the CRC verification algorithm to ensure the correctness and integrity of data transmission.

The principle of CRC verification is simple and clear, and it has the advantages of simple implementation and easy hardware implementation. It adds a checksum to the data frame, so that the receiver can detect whether the data frame has an error during transmission through simple division operations.

5.2 Function list

5.2.1 Main characteristics

The CRC module includes programmable polynomial settings that support commonly used CRC standards:

- CRC polynomial widths of 8, 16, 24, and 32 bit are supported
- The initial CRC value is all 0 or all 1
- Supports bitwise reversal of each byte of input data.
- Before supporting XOR output, the entire data is inverted bitwise by CRC width
- Support CRC result variance or output
- CRC results can be stored in the data tail or CRCVAL register
- CRC encoding and decoding are supported
- DMA is used for data migration, and CRC operations are performed at the same time as the migration

Note:

1. Only one DMA channel can be opened for CRC calculation at the same time.

5.2.2 Typical CRC parameter model

Name	PolyLen	Poly	InitialVal	DatEndian	XorOut	Generatorpolyno-mial
CRC-8	8	0x07	0x00	FALSE	0x00	$x^8+x^2+x^1+1$
CRC-8/ROHC	8	0x07	0xFF	TRUE	0x00	$x^8+x^2+x^1+1$
CRC-8/MAXIM	8	0x31	0x00	TRUE	0x00	$x^8+x^5+x^4+1$
CRC-16/IBM	16	0x8005	0x0000	TRUE	0x0000	$x^{16}+x^{15}+x^2+1$
CRC-16/MAXIM	16	0x8005	0x0000	TRUE	0xFFFF	$x^{16}+x^{15}+x^2+1$
CRC-16/USB	16	0x8005	0xFFFF	TRUE	0xFFFF	$x^{16}+x^{15}+x^2+1$
CRC-16/MODBUS	16	0x8005	0xFFFF	TRUE	0x0000	$x^{16}+x^{15}+x^2+1$
CRC-16/CCITT	16	0x1021	0x0000	TRUE	0x0000	$x^{16}+x^{12}+x^5+1$

CRC-16/CCITT-FALSE	16	0x1021	0xFFFF	FALSE	0x0000	$x^{16}+x^{12}+x^5+1$
CRC-16/X25	16	0x1021	0xFFFF	TRUE	0xFFFF	$x^{16}+x^{12}+x^5+1$
CRC-16/XMODEM	16	0x1021	0x0000	FALSE	0x0000	$x^{16}+x^{12}+x^5+1$
CRC-32	32	0x04C11DB7	0xFFFFFFFF	TRUE	0xFFFFFFFF	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x8+x^7+x^5+x^4+x^2+x^1+1$
CRC-32/MPEG-2	32	0x04C11DB7	0xFFFFFFFF	FALSE	0x00000000	$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x^1+1$

Table 5.1: Typical parametric models

Name: The name of the CRC model.

PolyLen: CRC polynomial width.

Poly: Shorthand for polynomial generation terms, expressed in hexadecimal. For example, CRC-16/X25 generates a polynomial of $x^{16}+x^{12}+x^5+1$, and the complete generating term is 0x11021, ignoring the highest "1", and the polynomial is abbreviated as 0x1021.

InitialVal: The CRC initializes the preset value.

DatEndian: FALSE means that each byte of input data is not reversed bitwise (MSB takes precedence), and the output calculation result is not reversed bitwise; TRUE means that each byte of input data is reversed bitwise (LSB first); The output is reversed bitwise (Note: the calculation is reversed bitwise on the PolyLen width).

XorOut: The result is calculated with the value of the PolyLen width (all 0 or all 1) and then output.

5.2.3 CRC calculation flow chart

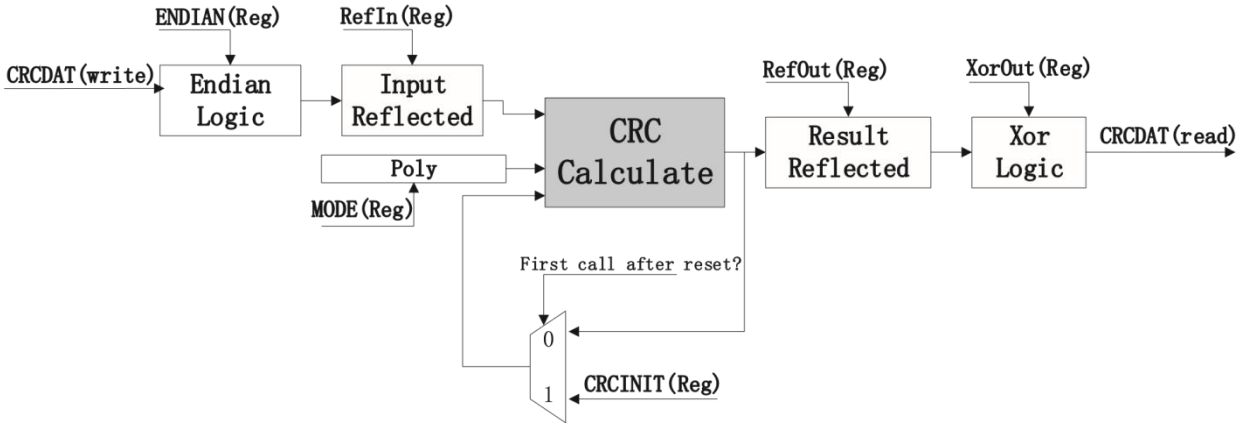


Figure 5.1: Calculation flow chart

6. ADC module

6.1 Overview

DCADC (Direct Current Analog to Digital Converter) module, that is, DC ADC. The main function is to realize single-channel and multi-channel cyclic sampling, and automatically transmit the sample value to the specified memory space, and can automatically calculate RMS at the same time.

The DCADC module has 4 input ports, each with an independent sample enable control bit and an RMS calculation enable control bit. The DCADC module has a configurable sampling rate with a sampling accuracy of 12 bit and supports the original sampling value or automatic calculation of RMS.

6.2 List of functions

The main features of the module are as follows:

- Support 4 input ports
  - With independent channel enablement
  - Independent RMS calculation enablement
- Operating mode optional
  - Single or cyclic mode is available
  - Single or multi-channel optional
- 2 sample rates are available
  - Sampling rate 2KHz
  - Sampling rate 2.4KHz
- 2 output results are available
  - Output the original ADC value
  - Output RMS value
- The sampling accuracy is 12 bit

7. DEBUG module

7.1 Overview

- The DEBUG module provides a dedicated interface for external hosts to access internal chip resources, including SSPI and JTAG interfaces
- SSPI stands for Slave SPI, which allows external hosts to access the chip through the SSPI interface, and all requests are made through 4 indirect addressing registers
- JTAG stands for Joint Test Action Group, which allows external hosts to implement online programming, online debugging, etc. through the JTAG interface

8. DMA module

8.1 Overview

DMA modules provide high-speed data transfer between peripherals and RAM or between RAM and RAM, and do not require CPU involvement in the process of DMA data handling, thus greatly reducing the workload of the CPU.

8.2 List of functions

- The DMA module has a total of 12 independent configurable channels
- DMA transmission can be peripheral-to-RAM, RAM-to-peripheral, RAM-to-RAM, and FLASH-to-RAM
- Each channel supports up to 22 external request sources
- 12 channels can work simultaneously
- Configurable address increment mode (address increment based on bit width for data transfer)
    - Incremental mode
    - Fixed mode
    - Intra-block cyclic increment mode (block transfer mode only)
- Configurable address loop mode
    - Loop mode
    - Acyclic mode
- Configurable data transfer methods
    - Single transfer (one data transfer at a time)
    - Block transfer (transfer of entire blocks of data in one request)
- DMA supports 3 types of interrupts:
    - The transmission is interrupted
    - Semi-transmission interruption
    - Transmission error interruption
- Configurable data transfer bit width
    - 8 bit
    - 16 bit
    - 32 bit
- CRC Engine is supported
- AES Engine is supported
- Support SM4 Engine

9. ECC module

9.1 Overview

ECC (Elliptic Curve Cryptography) is an asymmetric encryption algorithm based on discrete logarithmic computation problems on elliptic curves, which provides a secure way to perform cryptographic operations such as key exchange, digital signatures, and encryption.

The encryption protocols or algorithms supported by this module include ECDSA (EC Digital Signature Algorithm), SM2 (SM2 Elliptic Curve Public Key Cryptography Algorithm), and related variant protocols.

9.2 List of functions

- Support 3 elliptic curves
  - SECP256R1
  - BRAINPOOL_P256R1
  - SECP384R1

- Support 2 encryption modes
  - ECC
  - SM2

- Support 5 types of large numeric and analog operations
  - ModularPlus
  - ModularSubtract
  - ModularMultiply
  - ModularDivision
  - ModularInverse

- Support 3 types of point operations
  - DotMultiply
  - DotAdd
  - DotVerifyOnCurve

- ECDSA/SM2 signature/authentication operations are supported
  - ECDSASign
  - ECDSAVerify
  - SM2Sign
  - SM2Verify

10. EXTI module

10.1 Overview

The Cortex-M4® integrates a Nested Vectored Interrupt Controller (NVIC) for efficient exception and interrupt handling. NVIC enables low-latency exception and interrupt handling, as well as power management control. It is tightly coupled with the kernel.

For more information on NVIC, please refer to 《Cortex-M4® Technical Reference Manual》.

The functions of the EXTI (Interrupt Controller) module include the function of selecting interrupt event requests as input to, selecting interrupt event requests as interrupts to input to NVIC, waking up WFI; Wake up WFE by selecting the interrupt event request as the event input.

10.2 List of functions

- Support 1 set of power loss interrupts
  - Independent interrupt enable control
  - Separate interrupt flags and status bit
- Supports up to 49 GPIO interrupts
  - Support level triggering
  - Supports edge triggering
  - With independent interrupt shielding bit
- Support 6 sets of TIMRE interrupts
- Supports 6 sets of STIMER interrupts
- Support 6 groups of UART interrupts
- Support 2 sets of HPLC interrupts
- Support 2 sets of PWM interrupts
- Support 1 set of SPI interrupts
- Support 1 set of QSPI interrupts
- Support 1 set of SSPI interrupts
- Supports 2 I2C interrupts
- Support 1 set of I2S interrupts
- Support 1 set of ECC interrupts
- Support 1 set of AES interrupts
- Support 1 set of RTC interrupts
- Support 1 set of DCADC interrupts
- Support 1 set of PLL lock interrupts
- Support 1 set of DMA interrupts

11. GPIO module

11.1 Overview

1. Up to 49 general-purpose I/O pins are supported, from GPIO0–GPIO48, which are used by various on-chip devices to implement logic input/output functions.
2. Each GPIO port has associated control and configuration registers to meet the needs of specific applications.
3. Each GPIO port supports input, output, interrupt, and multiplexing functions.
4. External interrupts on GPIO ports have configuration registers associated with the interrupt controller (EXTI) that support level triggering (high/low) and edge triggering (rising/falling edges).
5. GPIO ports can be configured as peripherals for maximum flexibility in specific packages.

11.2 Feature list

11.2.1 Main features

- Each pin has input/output direction control
- Each pin has an internal weak pull-up function
- Each pin supports a push-pull output, with 5 pins supporting an open-drain output
- Each pin supports external interrupt triggering
- Some pins can be used as multiplexing functions for peripherals

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Note:

1. If the pin is configured as an output, the internal weak pull-up function is invalid.

11.2.2 Pins that support open-drain output

There are 5 pins that support open-drain output.

Table 11.1: Open Drain Output Pins

Pin name
RGPIO5 RGPIO23 RGPIO35 RGPIO36 RGPIO38

11.2.3 Support for STMR capture pins

There are 12 pins that can be used as an input capture function for STMR, supporting rising edge triggering.

Table 11.2: STMR capture pins

Pin name
RGPIO7 RGPIO8 RGPIO9 RGPIO10 RGPIO15 RGPIO16 RGPIO25 RGPIO26 RGPIO27 RGPIO28 RGPIO35 RGPIO36

11.2.4 Pin multiplexing function

Table 11.3: Multiplexing Functions

Name	48PIN	64PIN	72PIN	DEF_FUNC	FUNC0	FUNC1	FUNC2	FUNC3
RGPIO34	/	PIN8	PIN9	GPIO	I2C1_SCL	PWM6-P		
RGPIO33	/	PIN9	PIN10	GPIO	I2C1_SDA	PWM6-N		
RGPIO36	PIN8	PIN10	PIN11	GPIO	I2C0_SDA			
RGPIO35	PIN9	PIN11	PIN12	GPIO	I2C0_SCL			
RGPIO42	/	PIN12	PIN14	GPIO				
RGPIO10	PIN10	PIN13	PIN15	GPIO	MSPI3_MI	GPIO	DC_IN_3	
RGPIO7	PIN11	PIN14	PIN16	GPIO	MSPI3_MO	GPIO	DC_IN_4	
RGPIO8	PIN12	PIN15	PIN17	GPIO	MSPI3_SCK	GPIO	DC_IN_1	
RGPIO9	PIN13	PIN16	PIN18	GPIO	MSPI3_CSN	GPIO	DC_IN_2	
RGPIO39	PIN14	PIN17	PIN19	GPIO	UART3_TX	PWM4-P		
RGPIO40	PIN15	PIN18	PIN20	GPIO	UART3_RX	PWM4-N		
RGPIO22	/	PIN19	PIN21	GPIO	MSPI1_MI	I2S_DO		
RGPIO19	/	PIN20	PIN22	GPIO	MSPI1_MO	I2S_DI		
RGPIO20	/	PIN21	PIN23	GPIO	MSPI1_SCK	I2S_BCLK		
RGPIO21	/	PIN22	PIN24	GPIO	MSPI1_CSN	I2S_LRCLK		
RGPIO23	PIN18	PIN25	PIN28	GPIO	MCU_CLK	OSC_CLK	TMR2_CAP	I2S_MCLK
RGPIO24	PIN19	PIN26	PIN29	WEN	WEN	GPIO		
RGPIO0	/	PIN27	PIN30	GPIO	GPIO			
RGPIO1	/	PIN28	PIN31	GPIO	GPIO			

RGPIO25	PIN20	PIN29	PIN32	JTAG_TMS	JTAG_TMS	MSPI1_MO	GPIO	I2S_DI
RGPIO26	PIN21	PIN30	PIN33	JTAG_TDI	JTAG_TDI	MSPI1_SCK	GPIO	I2S_BCLK
RGPIO27	PIN22	PIN31	PIN34	JTAG_TDO	JTAG_TDO	MSPI1_CSN	TMR3_CAP	I2S_LRCLK
RGPIO28	PIN23	PIN32	PIN35	JTAG_TCK	JTAG_TCK	MSPI1_MI	GPIO	I2S_DO
RGPIO15	PIN24	PIN33	PIN36	GPIO	UART2_TX	GPIO	PWM1	
RGPIO16	PIN25	PIN34	PIN37	GPIO	UART2_RX	GPIO	PWM2	
RGPIO29	PIN26	PIN35	PIN38	SSPI_SO	SSPI_SO	SPI0_MOSO	IFDI	
RGPIO32	PIN27	PIN36	PIN39	SSPI_SI	SSPI_SI	SPI0_MISI	IFDI	
RGPIO30	PIN28	PIN37	PIN40	SSPI_SCK	SSPI_SCK	SPI0_SCK	IFDI	
RGPIO31	PIN29	PIN38	PIN41	SSPI_CSN	SSPI_CSN	SPI0_CSN	IFDI	
RGPIO43	/	PIN42	PIN45	GPIO	UART5_TX			
RGPIO44	/	/	PIN46	GPIO	UART5_RX			
RGPIO45	/	/	PIN47	GPIO	UART4_TX			
RGPIO46	/	/	PIN48	GPIO	UART4_RX			
RGPIO2	/	PIN43	PIN49	GPIO	TMR1_CAP			
RGPIO3	/	PIN44	PIN50	GPIO				
RGPIO47	/	/	PIN51	GPIO				
RGPIO48	/	/	PIN52	GPIO				
RGPIO17	PIN33	PIN45	PIN53	GPIO	UART1_TX	GPIO	PWM3	TMR4_CAP
RGPIO18	PIN34	PIN46	PIN54	GPIO	UART1_RX	GPIO	TMR5_CAP	PWM0
RGPIO38	PIN35	PIN47	PIN55	GPIO		UART0_TX		
RGPIO37	PIN36	PIN48	PIN56	GPIO		UART0_RX		
RGPIO14	/	PIN49	PIN57	GPIO	MSPI2_MI	I2S_DO		
RGPIO11	/	PIN50	PIN58	GPIO	MSPI2_MO	I2S_DI		
RGPIO12	/	PIN51	PIN59	GPIO	MSPI2_SCK	I2S_BCLK		
RGPIO13	/	PIN52	PIN60	GPIO	MSPI2_CSN	I2S_LRCLK		
RGPIO4	PIN37	PIN53	PIN61	GPIO	GPIO		PWM5-P	
RGPIO5	PIN38	PIN54	PIN62	GPIO	TMR0_CAP	I2S_MCLK	PWM5-N	
RGPIO41	PIN41	PIN57	PIN65	GPIO				
RGPIO6	PIN42	PIN58	PIN66	GPIO	TX_BUSY			

11.2.5 Pins to Note

1. RGPIO24

   This pin is used to automatically enable the watchdog timer.

When the MCU reset starts, it automatically detects the high and low status of the pin: if it is high, it forces the watchdog to start; If it is low, the watchdog will not be started, and the watchdog can be started by the software later.

2. RGPIO25，RGPIO26，RGPIO27，RGPIO28

   These pins are used to control JTAG download and emulation; If you need to connect a debugger, the pins must remain JTAG multiplexed.

3. RGPIO29,RGPIO30,RGPIO31,RGPIO32

   These pins are used to download programs through the SSPI interface, which cannot be downloaded if configured in other modes.

   Therefore, when you need to download a program, the software needs to configure these pins to SSPI mode.

11.3 Electrical characteristics

To be added.

12. I2C module

12.1 Overview

- The I2C module provides a serial interface that complies with the Philips I2C bus specification, using two buses to realize data transmission between the device and the bus, and the status register I2cSta reflects the transmission status of the I2C bus controller in real time during the transmission process.
- I2C is a synchronous half-duplex serial communication interface that uses two wires to transmit data between the device and the bus: the serial clock SCL and the serial data SDA.
- Every device connected to the bus has a unique address.
- I2C is a true multi-master bus that includes collision detection and arbitration mechanisms to prevent data loss when multiple hosts begin data transfer simultaneously.

12.2 List of functions

- There is only one I2C communication interface, which supports master-slave mode
- Supports I2C synchronous half-duplex serial communication protocol
- The supported I2C communication rate is adjustable
- Support 7-bit address mode
- When in master mode, a programmable clock generator supports serial clocking
- When in slave mode, the internal clock generator is turned off, using the serial clock provided by the external host
- When a change in the bus state is detected, an I2C interrupt can be generated if the I2C interrupt is enabled
- It supports SCL and SDA open-drain modes, and the external hardware pull-up resistor realizes the "line and" logic of the signal

13. I2S module

13.1 Overview

I2S (Inter-IC Sound) bus is a bus standard developed by Philips for audio data transmission between digital audio devices, which is dedicated to data transmission between audio devices and is widely used in various multimedia systems.

The I2S module supports I2S/PCM mode, full-duplex/half-duplex communication, master/slave mode setting, DMA data transmission, etc.

13.2 List of functions

- Support I2S/PCM mode
- Supports full-duplex/half-duplex communication
- Support master/slave mode settings
- Supports dual channels
- Support 2/4 channels
- DMA data transfer is supported
- Channel bit width and length are configurable
  - 8bit
  - 16bit
  - 24bit
  - 32bit
- Data bit width and length are configurable
  - 8bit
  - 16bit
  - 24bit
  - 32bit
- The sample rate is configurable
- Support for the main clock output function (via CLKOUT) pin

14. MEMORY module

14.1 Overview

14.1.1 FLASH

- The flash is stacked and has a maximum capacity of 1MB
- Read, write, sector erase, and full erase operations are supported
- The sector size of sector erasure is 4KB
- Support 8-bit data reading
- 32-bit data can be written, and 32-bit writes must be done

14.1.2 SRAM

- The memory capacity is 384KB and can be accessed by 8-bit, 16-bit, and 32-bit
- Read and write operations are performed on the CPU clock, with no waiting periods
- SRAM can execute code

15. MSPI module

15.1 Overview

MSPI (Master Serial Peripheral Interfacer) module, that is, an SPI module that can only be used as a host mode, is mainly used to communicate with slaves with SPI standard interfaces.

The chip includes 3 MSPI interfaces, all of which are derived from external pins, to communicate with slaves with SPI standard interfaces.

15.2 List of functions

The main features of the module are as follows:

- Read/FastRead/PageProgram commands are supported
- Only SPI Master mode is supported
- Data transfer is variable or configurable
- Programmable clock phases
- Programmable clock polarity

16. PMU module

16.1 Overview

PMU (Power Management Unit) is the power management module of the chip, and its functions are as follows:

- The internal LDO provides 1.0V power to the chip digital module.
- The system power supply is monitored, and BOR and POR reset signals are generated according to the voltage amplitude of the AVDD3P3.

16.2 List of functions

- The chip DVDD1P0 is digitally powered, and can be controlled by internal or external infusion.
- The chip has built-in AVDD1P2 and DVDD1P2
- Independent PLC power supply
- Independent clock power supply
- Built-in power detection module, which can output POR or BOR reset according to AVDD3P3 voltage

16.3 PMU Electrical Specifications

16.3.1 POR

Table 16.1: POR electrical parameters

	MIN	TYP	MAX	unit
Power-up flip threshold		2.8		V
Power-down flip threshold		2.8		V
Analog filtering		2		ms
Power consumption				nA

16.3.2 BOR

Table 16.2: BOR electrical parameters

	MIN	TYP	MAX	unit
Power-up flip threshold		2.4		V
Power-down flip threshold		2.4		V
Analog filtering				us
Power consumption				nA

16.3.3 LDO

16.3.3.1 DVDD1P0

Table 16.3: DVDD1P0 Electrical Parameters

	MIN	TYP	MAX	Unit
Operating voltage	2.8	3.3	3.6	V

Output voltage		1.00		V
Establishment time				us
Quiescent consumption				mA
Linear modulation				mV/V
Load modulation				mV/mA
Voltage stabilization capacitors		4.7		uF

16.3.3.2 DVDD1P2

Table 16.4: DVDD1P2 Electrical Parameters

	MIN	TYP	MAX	Unit
Operating voltage	2.8	3.3	3.6	V
Output voltage		1.20		V
Establishment time				us
Quiescent consumption				mA
Linear modulation				mV/V
Load modulation				mV/mA
Voltage stabilization capacitors		4.7		uF

16.3.3.3 AVDD1P2

Table 16.5: AVDD1P2 electrical parameters

	MIN	TYP	MAX	Unit
Operating voltage	2.8	3.3	3.6	V
Output voltage		1.20		V
Establishment time				us
Quiescent consumption				mA
Linear modulation				mV/V
Load modulation				mV/mA
Voltage stabilization capacitors		0.1		uF

17. PWM module

17.1 Overview

PWM (Pulse Width Modulation) control is a technology that modulates the width of a pulse, that is, by modulating the width of a series of pulses, the required waveform is equivalently obtained.

17.2 List of functions

17.2.1 Main characteristics

- Support 6 PWM channels, controlled by two timer IPs respectively, with each timer IP independently controlling its dedicated 2 PWM channels.
- Support independent output and dual simultaneous output
- The dual simultaneous output function supports synchronous output mode and complementary output mode
- The complementary output mode supports dead-time insertion function
- Both the counter and the comparator have a bit width of 16 bit
- Support three counting methods: up counting, down counting, and central counting
- Support frequency and duty cycle adjustable
- Count based on MAC clock

18. QSPI module

18.1 Overview

The QSPI module is specially used to control Flash to protect the accuracy and completeness of Flash content, avoid abnormal modification of Flash content, and improve the efficiency of Flash operation.

The QSPI module supports adjusting the clock frequency divider ratio to adapt to different application scenarios.

The QSPI module also integrates cache-related functions.

18.2 Feature List

- Support clock frequency divider ratio configurable
- Support reading, writing, erasing, and other operations on Flash
- Support reading and writing SR registers to Flash
- Support obtaining Flash id
- Supports statistics on Cache hit and miss
- Support address remapping function

19. RESET module

19.1 Overview

The system supports a variety of reset methods, which are divided into the following types:

- Power reset
  - Power-on detection reset (POR_RST)
  - Power Loss Detection Reset (BOR_RST)
- System reset
  - External Pin Reset (PIN_RST)
  - Watch Dog Reset (WDT_RST)
  - Software Reset (SOFT_RST)

When any reset source generates a reset, the MCU's program pointer reverts to 0000H, all chip registers revert to the reset default, and the external pin level reverts to the reset state.

19.2 List of functions

The system supports reset as follows:

- Power-on detection reset (POR_RST)
- Power Loss Detection Reset (BOR_RST)
- External Pin Reset (PIN_RST)
- Watch Dog Reset (WDT_RST)
- Software Reset (SOFT_RST)

20. RTC module

20.1 Overview

The RTC (Real Time Clock) module, or real-time clock module, has a set of continuously counted counters inside that provide a clock calendar to the system.

The RTC module provides a perpetual calendar function with date (year/month/day/week) and time (hour/minute/second/subsecond).

The RTC module also has an alarm function. The alarm time can be set by software. When the set alarm time matches the value of the clock register, if the alarm interrupt enable is enabled, an alarm interrupt will be generated.

20.2 List of features

- Independent module enable switch
  - When enabled, the RTC counter starts counting.
  - When closed, the value of the clock register is stopped and retained.
- Perpetual calendar function is supported
  - The clock register contains the year/month/day/hour/minute/second/sub-second/week.
  - The minimum resolution is 100 milliseconds
- Support alarm clock function
  - The alarm time can be set independently, including month/day/hour/minute/second/sub-second/week.
  - Alarm setting time, month/day/hour/minute/second/sub-second/week all have independent comparison enable control.
  - When the time register matches the set alarm time, an alarm event can be generated.
  - The alarm clock generation mode can be set, and it supports the generation of alarm clock events per year/month/day/hour/minute/second/week.
- With a high-precision clock source
  - The RTC clock source is obtained by the clock division of an external high-frequency oscillator.
  - The RTC clock frequency is 32.768KHz
- It has independent interrupt enablement
  - Interrupt enable configurable
- Support dual time formats
  - 12-hour tense
  - 24-hour tense system
- Support AM or PM selection

Note: 1. The AM or PM selection setting is valid only if the HourFormat is 1.

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21. SM2 module

21.1 Overview

The national secret SM2 algorithm is an asymmetric elliptic curve algorithm, which provides efficient and secure digital signature and public key algorithms based on elliptic curves.

- Security: The SM2 algorithm is based on the mathematical puzzle of elliptic curves, providing higher security compared to traditional public-key algorithms such as RSA.
- Efficiency: The SM2 algorithm requires shorter key lengths and higher computational efficiency under the same security level.
- Compliance: As a national standard, the SM2 algorithm has been widely promoted and applied in Chinese government agencies, financial industries, and other fields.

21.2 List of features

- Elliptic curves that support national secret standards
  - SM2
- Support 5 types of large numeric and analog operations
  - Modular Plus
  - Modular Subtract
  - Modular Multiply
  - Modular Division
  - Modular Inverse
- Support 3 types of point operations
  - Dot Multiply
  - Dot Add
  - Dot Verify On Curve
- SM2 signature/authentication operations are supported
  - SM2 Sign
  - SM2 Verify

Note:

1. The registers of the SM2 module are the same as the ECC module, please refer to the ECC register description.

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22. SM4 module

22.1 Overview

The SM4 algorithm is a symmetric encryption and decryption algorithm that uses the same key for encryption and decryption.

The key length is fixed at 128 bit.

The input data is grouped by 128-bit length, and if the length of the input data is not an integer multiple of 128-bit, it needs to be filled.

The output data length is equal to the input data length.

22.2 List of functions

- Fixed key length
  - 128bit
- Algorithm mode configurable
  - ECB mode
  - CBC mode
- Supports encryption or decryption operations
- Data size is configurable
- Support automatic key expansion: For encryption and decryption keys, multiple round keys will be generated internally through key expansion
- Use one DMA channel to input plaintext data and another DMA channel to output ciphertext data
- Encryption and decryption are supported to complete interruptions, but if DMA mode is used, no interrupts will occur

23. SPI module

23.1 Overview

The SPI (Serial Peripheral Interface) module, is the serial peripheral interface, provides data transmission and reception functions based on the SPI protocol, which can realize full-duplex synchronous serial communication with peripheral devices that have an SPI interface.

23.2 List of functions

The main features of the module are as follows:

- 3/4 line full duplex synchronous transmission
- 2/3 line half-duplex synchronous transmission
- Host/slave mode
- 7 types of host baud rates
- The communication clock is up to Fcpu/4
- 8-bit transmission frame format, MSB/LSB configurable
- Polarity and phase configurable
- Write conflict handling mechanisms
- Transmit and receive FIFO depths up to 64bytes
- Configurable FIFO interrupts

24. STIMER module

24.1 Overview

The Stimer module provides a 32-bit high-precision counter. Once powered on, the counter automatically starts counting from zero. It does not reset normally and continues to count until it overflows, after which it restarts counting.

Each stimer contains 2 comparators. When the value of the comparator is equal to the count value of the stimer, an interrupt can be generated or the TDP start can be triggered (only stimer 0 supports this).

Each stimer contains 1 capture to capture the time of change in the external input signal.

It supports frequency offset compensation function to realize automatic frequency tracking.

24.2 List of functions

- Support six Stimer modules
- 32-bit incremental counter
- A 16-bit pre-divider for crossing the counter clock frequency with a crossover factor between 1 and 65535
- 2 comparators
- 1 capture
- Supports frequency offset compensation function
- 5 working modes:
  - Counter mode
  - Comparator (i.e., periodic timing) mode
  - Input capture mode
  - TDP start mode (only stimer0 supported)
  - FCH latch mode (only stimer0 supported)
- The following interrupt requests are supported:
  - Input capture interruptions
  - Comparison (Periodic Timer) interruptions

25. TIMER module

25.1 Overview

The timer includes a 32-bit auto-reload counter driven by a programmable prescaler.

This timer can be used as a general-purpose timer to generate timebases, or to capture the timing of external inputs.

When the counter mode is enabled, the counter starts counting, with the counting frequency divided by TmrDiv.PreDiv. The current count value can be read from the TmrCnt.CntVal register.

When the periodic timer mode is enabled, if the value of the counter matches the written period value (TmrPrd.Prd) and TmrIE.PrdIE is set, the TmrIF.PrdIF interrupt will be triggered. (Note: This counter can only count up, not count down.)

When the capture mode is enabled, the module will capture rising or falling edges based on the configuration of TmrCtrl.CCMode. Upon detecting the corresponding event, the module automatically saves the current counter value to TmrCap.CapVal register. If TmrIE.CapIE is set, the TmrIF.CapIF interrupt will be generated.

25.2 List of features

- Support six Timer modules
- 32-bit incrementing / incrementing auto-reloading counter
- A 32-bit prescaler used for dividing the counter clock frequency, with a division coefficient ranging from 1 to (2^32 - 1).
- Three operating modes:
  - Counter mode
  - Input capture mode
  - Periodic timing mode
- The following interrupt requests are supported:
  - Input captures interruptions
  - Periodic Timer Interrupt

26. UART module

26.1 Overview

UART (Universal Asynchronous Receiver/Transmitter) provides a flexible method for exchanging full-duplex data with external devices using the industrial standard NRZ asynchronous serial data format. In addition to the standard asynchronous transceiver mode, UART also has an infrared modulation function to enable infrared communication.

The data bit, stop bit, check mode and logic levels can be flexibly configured. The transmit and receive FIFOs combined with DMA can achieve high-speed data communication.

26.2 List of functions

26.2.1 Main features

- Full-duplex asynchronous communication, supports 4 serial ports, and supports positive and negative logic for communication levels.
- The serial clock source is a MAC clock, and the baud rate can be matched, and the maximum speed can reach 2Mbps
- It supports infrared modulation output, the modulation polarity is configurable, and the infrared modulation frequency can be matched, and the default frequency is 38KHz
- Configurable data bit length
  - 7 bit
  - 8 bit
- Configurable stop bit
  - 1 bit
  - 2 bit
- Configurable Parity bit
  - Odd Parity
  - Even Parity
  - All 0
  - All 1
  - No Parity
- Receive and transmit can be independently enabled
- Independent receive/transmit FIFO with configurable maximum trigger depth of 16 bytes
- Serial port data Buffer with DMA request support

27. WDT module

27.1 Overview

The WDT (Watchdog Timer) is a special timer that generates an overflow pulse and triggers a watchdog reset when it counts up to its maximum value. If the WDT Counter is configured to a value less than its maximum value through WdtRldVal before the overflow pulse occurs, no watchdog reset will be generated.

27.2 List of functions

- The hardware dog design is adopted. When the WDTEN PIN is pulled high or the WdtEn position is 1, the watchdog is enabled. The default reset time of the WDT is 10 seconds, and the maximum reset time is 100 seconds.
- Once the WDT is enabled, it can only be turned off by pulling down the WDTEN PIN during the chip reset process.
- Based on the OSC clock division, the counting period is 100ms, a 10-bit incrementing counter, with a counting range of 0 to 1000. When the counter reaches 1000, the WDT is reset.
- By reloading the count value in the WdtRldVal register, the dog-feeding operation can be achieved. The range of the reloaded count value is 0 to 1000.