STT-MRAM Datasheet

PM256KNIA

Version:1.0

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Contents

1 Description

PM256K is a 256K Bit/32K Byte SPI interface non-volatile memory. The chip adopts advanced PMTJ STT-MRAM technology, supports single-line SI and SO independent interfaces, achieves up to 20MHz read and write transmission, and has no delay in writing. It has excellent reliability and more than 20 years of data retention time.

PM256K is an ideal solution for MCU to expand external memory. At the same time, due to the characteristics of fast throughput, few pins and small size, it has gradually become the choice of applications such as embedded, network switches, automobiles and the Internet of Things.

Features :

PMTJ STT-MRAM technology

- STT technology
- 256K Bit/32K Byte

SPI interface

- 10MHz @READ mode
- 20MHz @FAST READ mode
- 20MHz@WRITE mode, no delay in writing
- Support SPI Mode0 and SPI Mode3

Single voltage operation

- Typical Voltage VCC 2.7V~3.6V

Operation Temperature range

- -40℃~85℃

Data protection

- Write protection mode configured by BP0 and BP1 of SR0 register

Power consumption

- Standby current 300μA (Typical value)
- Working current 3mA (typical write current @10MHz)

Reliability

- Data retention >20years @85℃
- Write times 1E12

Package

- SOP8

Order specification

Part No	Density	Operating voltage range	Package	Devices per bag/reel	Maximum Program/Erase Cycles	Operating temperature	Data retention
PM256KNIA	256K Bit/ 32K Byte	2.7V~3.6V	SOP8	2500pcs/reel	1E12	-40℃~85℃	≥20years @85℃

2 Pin Configuration

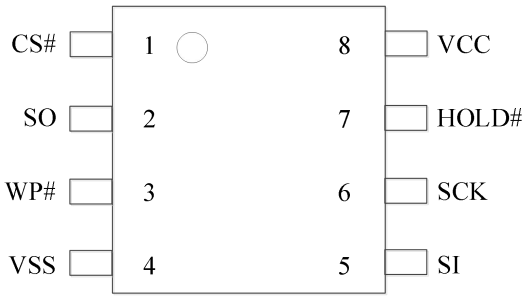


Figure 1: SOP8 Package Information (Top view)

Table1: Pin Description

No.	Symbol	Signal Type	Description
1	CS#	Input	Chip select enable signal
2	SO	Output	Serial output
3	WP#	Input	Write protection
4	VSS	Ground	Ground
5	SI	Input	Serial input
6	SCK	Input	Serial clock
7	HOLD#	Input	Hold
8	VCC	Power	Power supply

Pin function description:

(1) CS#: Chip select enable signal, low level enable; when CS# is high level, the chip does not work.

(2) SO: Serial data output pin, valid during read operation, data output occurs at the falling edge of serial clock SCK, when HOLD# is at "low" level or CS# is at "high" level, SO is in high-Z state, and remains in output state at other times.

(3) WP#: This is the pin that controls the write operation to the SR register, used in conjunction with WPEN.

(4) VSS: Ground pin.

(5) SI : Serial input pin, sampled at the rising edge of serial clock SCK.

(6) SCK: Clock input pin, provides clock signal for serial data input and output. Data of SI pin is input synchronously with the rising edge of SCK, and data of SO pin is output synchronously with the rising

edge of SCK. The chip supports SPI mode 0 (CPOL=0.CPHA=0) and SPI mode 3 (CPOL=1, CPHA=1). In mode 0, the clock is usually at a low level when idle. In mode 3, the clock is usually at a high level when idle.

(7) HOLD#: Hold pin. When it is at a low level, it will interrupt the current communication of the chip. SO becomes high-Z state, SCK and SI are in an ignorable state. The hold pin is pulled low only when CS# is low.

(8) VCC: Power supply voltage pin.

3 SR Register

The PM256K chip provides two SR registers, namely SR0 and SR1, which are stored in the internal register unit. Users can rewrite the SR0 register and SR1 register through register write instructions; the SR0 register status can be obtained through read instructions, but the chip does not support SR1 register read instructions.

The bit definition table of SR0 and SR1 is shown in Table 2.

Table 2: SR register bit allocation table

Register	Data bit definition							
	7	6	5	4	3	2	1	0
SR0	WPEN	RFU0	RFU1	RFU2	BP1	BP0	WEL	RFU3
SR1	RFU4	RFU5	RFU6	RFU7	BYTE_EN	RFU8	RFU9	RFU10

3.1 SR0 Register

In the SR0 register, WPEN (Bit7), BP1 (Bit3) and BP0 (Bit2) are readable and writable, RFU0 (Bit6), WEL (Bit1) and RFU3 (Bit0) are only readable, and RFU1 (Bit5) and RFU2 (Bit4) are reserved bits and do not participate in chip control. The default value of the SR0 register is 8'h01 after the chip is powered on and initialized.

After sending the write enable command, WEL (Bit1) becomes 1b'1; after sending the write disable command, WEL (Bit1) becomes 1'b0.

The main function of the SR0 register is to define the write protection mode. BP1 (Bit3) and BP0 (Bit2) define the protected area address range of the array, and the remaining address range is the non-protected area; WP#, WPEN (Bit7) and WEL (Bit1) combine to define how the write protection function is applied to the protected area, non-protected area and SR register.

Protected state: write operation fails.

Non-protected state: users can write normally.

Table 3: Protection zone address ranges

BP1	BP0	Protected area address range	
		32bit addressing	8bit addressing
0	0	No protected area	No protected area
0	1	0x1800-0x1FFF	0x6000-0x7FFF

1	0	0x1000-0x1FFF	0x4000-0x7FFF
1	1	0x0000-0x1FFF	0x0000-0x7FFF

Table 4: Write protection function

WEL (SR0)	WPEN (SR0)	WP# (PIN)	SR Register	Protected Areas	Non-protected areas
0	X	X	Protected status	Protected status	Protected status
1	0	X	Unprotected status	Protected status	Unprotected status
1	1	0	Protected status	Protected status	Unprotected status
1	1	1	Unprotected status	Protected status	Unprotected status

3.2 SR1 Register

All bits of the SR1 register are write-only bits. The default value is 8'h00 after the chip is powered on and initialized.

RFU4 (bit7), RFU5 (bit6), RFU6 (bit5), RFU8 (bit2), RFU9 (bit1) and RFU10 (bit0) are reserved bits that do not participate in chip control.

RFU7 (bit4) is a writable reserved bit. To make the chip work properly, the user needs to write 0 to bit4.

BYTE_EN (bit3) is a writable bit. When BYTE_EN=1, the chip is in 8-bit addressing mode. When BYTE_EN=0, the chip is in 32-bit addressing mode.

4 Chip Functions

According to the SPI protocol, the first 8 bits of input data are COMMAND (command code), which defines what operations the chip will perform. Depending on the command code, it may be followed by a 3-byte address, plus an idle clock cycle and a data byte, or it may be followed directly by a data byte.

The 24-bit (3-byte) address portion after some command codes defines the address that the chip will access; for an array with a capacity of 256Kb, the effective address is 13 bits in 32-bit addressing mode and 15 bits in 8-bit addressing mode.

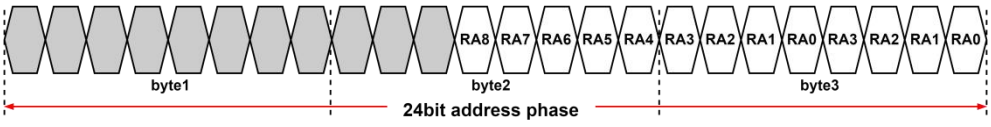


Figure 2: Schematic diagram of effective address (32-bit addressing mode)

Note:

1. All commands, addresses and virtual bits of the HS256K3SD device are shifted with the most significant bit first, and data bits are also shifted in or out with the most significant bit.

2. To avoid partial access to the chip, the user must keep CS# valid within multiples of 8 clocks after CS# goes low.

The functional operations supported by the chip are shown in Table 5.

Table 5: Chip Function Table

Commands	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7~
Write Enable	06h						
Write Disable	04h						
Normal Read	03h	A23 -A0			D31-D0 (until CS# is pulled high)		
Fast Read	0Bh	A23 -A0			Dummy	D31-D0(until CS# is pulled high)	
Write	02h	A23 -A0			D31-D0(until CS# is pulled high)		
SR0 Register Write	01h	S7-S0					
SR0 Register Read	05h	S7-S0					
SR1 Register Write	31h	S7-S0					
Enter Sleep Mode	B9h						
Exit Sleep Mode	ABh						
Read MANU ID	9Fh	ID7~ID0					
Read DEVICE ID	90h	ID7~ID0					
Read UNIQUE ID	4Bh	ID87~ID0					
Reset Enable	66h						
Reset	99h						

4.1 Write Enable and Write Disable

The function of the write enable command is to allow the subsequent write commands sent by the user, the SR0 register write command and the SR1 register write command to take effect; the function of the write disable command is to prevent the subsequent write commands sent by the user, the SR0 register write command and the SR1 register write command from taking effect. After sending the write enable command, the write enable latch bit WEL of the SR0 register is automatically set to 1. After sending the write disable command, the write enable latch bit WEL of the SR0 register is automatically set to 0.

The timing diagrams of the write enable and write disable commands are shown in Figures 3 and 4. First, pull down CS#, then send the 8-bit command code, and then pull up CS# to complete the command sending.

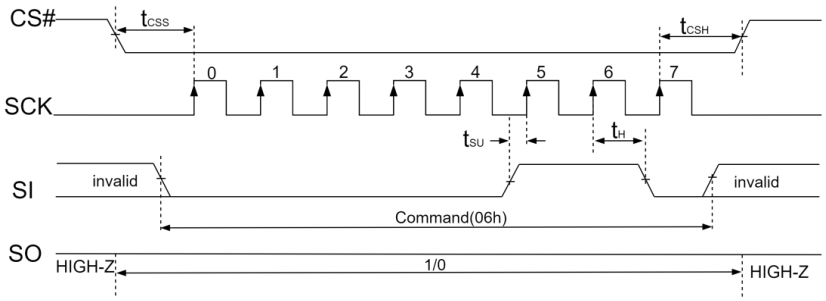


Figure 3: Write Enable Timing Diagram

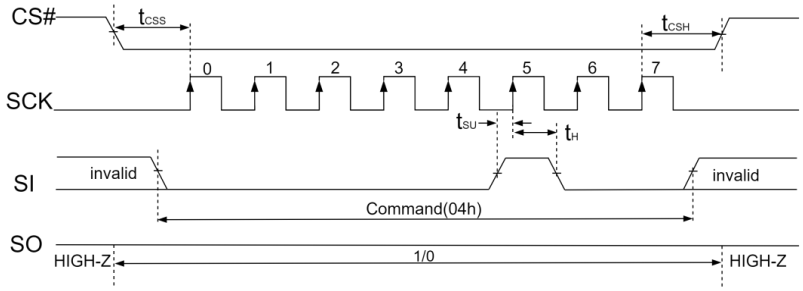


Figure 4: Write inhibit timing diagram

4.2 Normal read operation

The normal read command allows data to be read from the location specified by the 24-bit address. If CS# remains low and SCK is flipped, the user can continue to receive read data after receiving the first data, the address automatically increments, and the chip reads the data in the following addresses in sequence; when the address reaches the maximum address of the chip, the next address will scroll to the chip starting address 00h, and the data of the entire chip will be read in an infinite loop until CS# is pulled high to terminate the read operation.

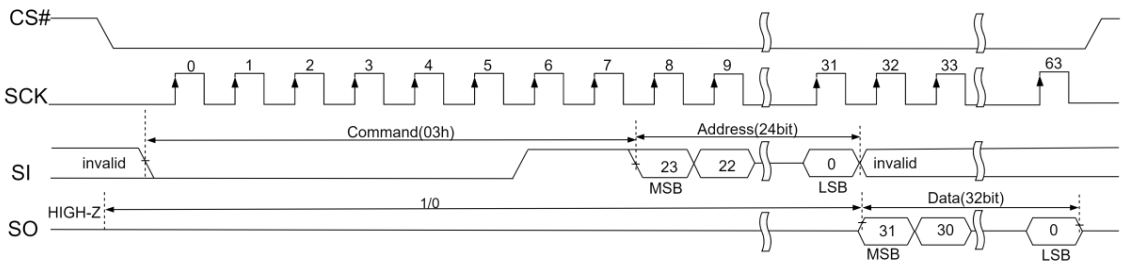


Figure 5: Read Operation Timing Diagram

4.3 Fast Read Operation

The fast read command allows data to be read from the location specified by the 24-bit address. If CS# remains low and SCK keeps flipping, the user can continue to receive read data after receiving the first data, the address automatically increments, and the chip reads the data in the following addresses in sequence; when the address reaches the maximum address of the chip, the next address will roll to the chip start address 00h, and the data of the entire chip will be read in an infinite loop; until CS# is pulled high to terminate the read operation.

The fast read command has similar functions to the normal read command, except that the normal read command supports up to 10MHz access, while the fast read command supports up to 20MHz access. The fast read instruction timing is shown in Figure 6, where dummy occupies 8 SCK.

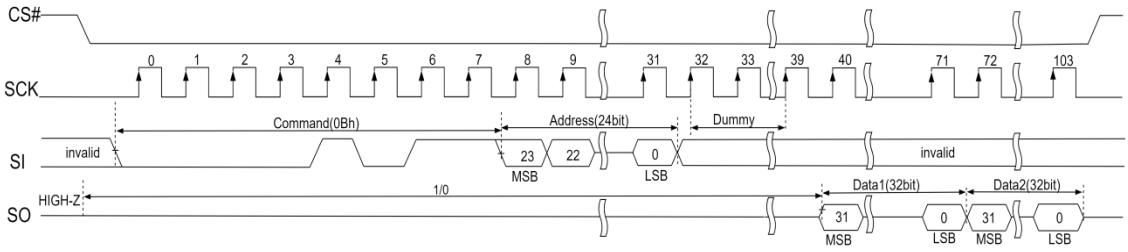


Figure 6: Fast Read Operation Timing Diagram

4.4 Write Operation

The write command allows data to be written from the location specified by the 24-bit address. If CS# remains low and SCK keeps flipping, the user can continue to send write data after the first data is sent, and the chip will write the data to the subsequent addresses in sequence; when the address reaches the maximum address of the chip, the next address will roll to the chip start address 00h, and write data to the entire chip in an infinite loop; until CS# is pulled high to terminate the write operation. The data written first in the same address will be overwritten by the subsequent data written.

Before performing a write operation, it is necessary to ensure that it is in the write enable state (WEL=1 of the SR0 register). The write operation timing is shown in Figure 7.

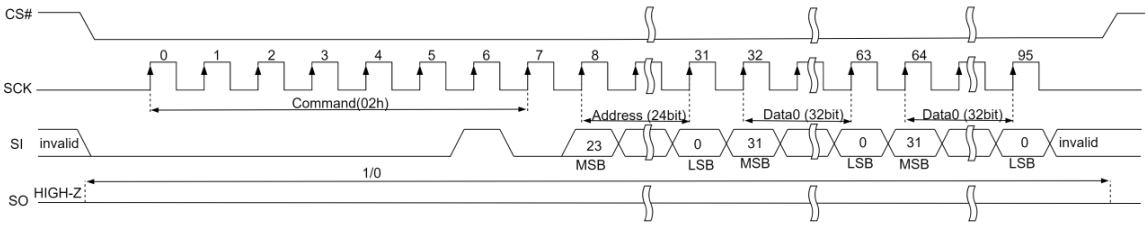


Figure 7: Write operation timing diagram

Note: If the user sends a write command (02h) and write address after CS# goes low, at least one write data must be sent before CS# is pulled high.

4.5 SR0 register read operation

The SR0 register read instruction allows reading the value of the SR0 register and obtaining the status of WPEN, BP1, BP0 and WEL. The SR0 register read instruction timing is shown in Figure 8.

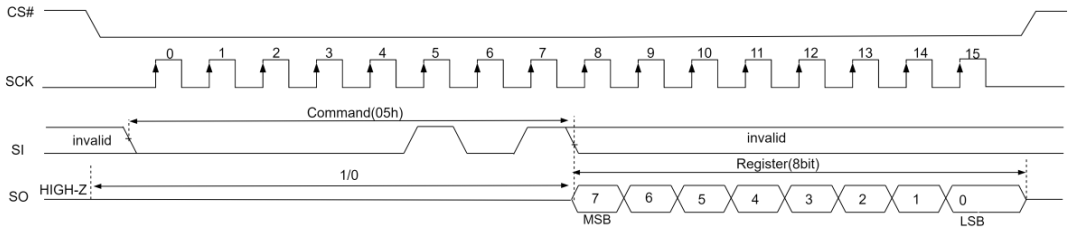


Figure 8: SR0 register read command timing diagram

4.6 Register Write Operation

The SR register write command allows new values to be written to the SR0 and SR1 registers. The commands are 01h and 31h respectively. The SR0 register write command timing and the SR1 register write command timing are shown in Figure 9 and Figure 10. The execution of the SR register write command requires the execution of the write enable command first, setting WEL to 1, and setting the WP# pin and WPEN values as shown in Table 4, so that the SR register is in a writable state.

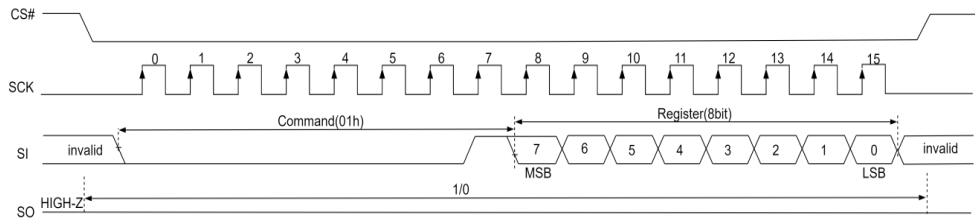


Figure 9: SR0 register write command timing diagram

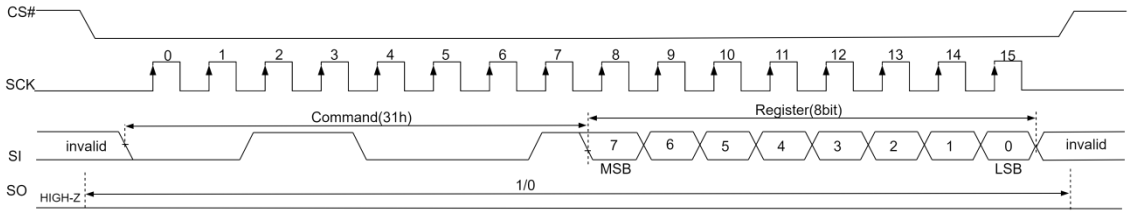


Figure 10: SR1 register write command timing diagram

4.7 Read ID Operation

This chip supports reading MANU ID, DEVICE ID and UNIQUE ID operations.

It should be noted that the read ID instruction is invalid in the following 3 cases:

1. 8-bit addressing mode (SR1 register is 0x08);

2. After performing a reset operation through a reset command (sending 66h, 99h commands);

3. Entering sleep mode and then exiting sleep mode (sending B9h, ABh commands). Therefore, it is recommended that users perform the read ID operation first after powering on, and then perform other operations.

The MANU ID of this chip is 8 bits in total, which can be read through a command (9Fh). After sending the 8-bit command code, the user can receive the MANU ID, which is 26h.

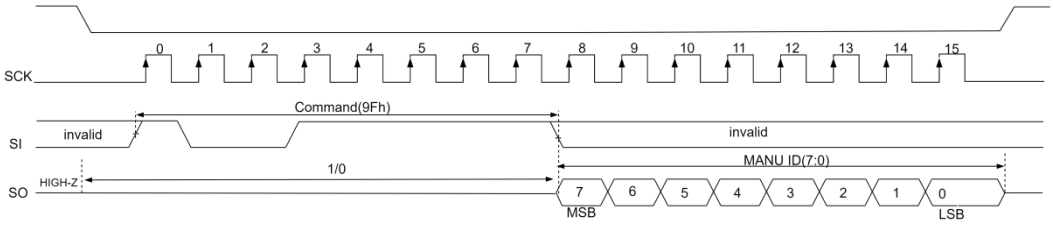


Figure 11: Read MANU ID command timing diagram

The DEVICE ID of this chip is 8 bits in total and can be read through the command (90h). After sending the 8-bit command code, the user can receive the DEVICE ID. The DEVICE ID is 29h.

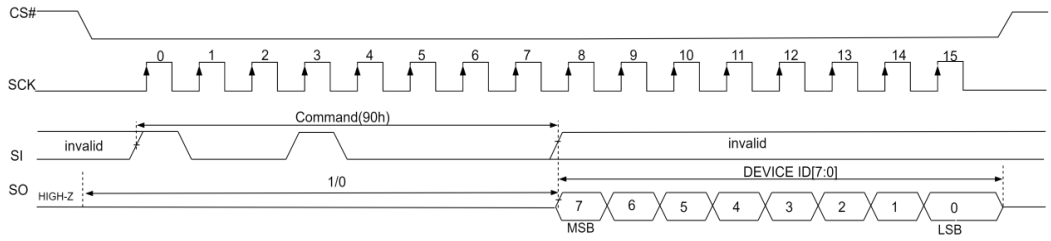


Figure 12: Read DEVICE ID command timing diagram

The UNIQUE ID of this chip is 88 bits in total and can be read through the command (4Bh). After sending the 8-bit command code, the user can receive the UNIQUE ID.

Table 6: UNIQUE ID command timing diagram

CMD	Byte1	Byte2	Byte3~Byte4	Byte5~Byte12
UNIQUE ID	4BH	0H	7F7FH	ID63~ID0

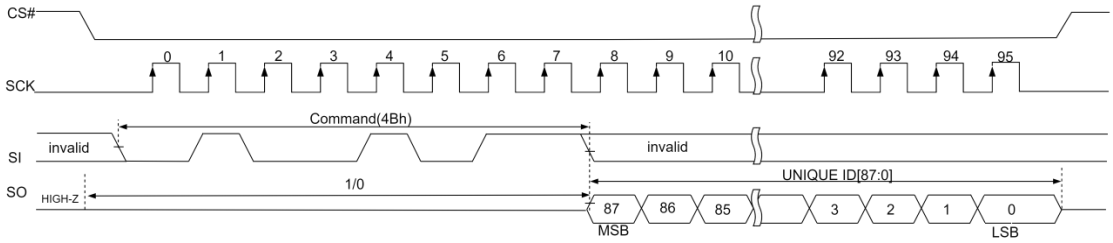


Figure 13: Read UNIQUE ID command timing diagram

4.8 Hold Function

The HOLD# pin is used to suspend the serial communication of the chip and realize the hold function. When the chip is selected and serial communication is in progress, the HOLD# pin can suspend the serial communication between the chip and the user without the user resetting the ongoing serial sequence. When the user needs to suspend communication, just pull down the HOLD# pin when the SCK pin is low; when the user needs to resume communication, just pull up the HOLD# pin when the SCK pin is low. During the period when HOLD# is low, SCK is allowed to flip. When the communication between the chip and the user is suspended, the input value on the SI pin will be ignored and the SO pin will be in a high impedance state.

It should be noted that if the pin is pulled low during the period when the CLK pin is low, the HOLD# pin needs to be returned to a high level during the period when the CLK pin is low; if the HOLD# pin is pulled low during the period when the CLK pin is high, the HOLD# pin needs to be returned to a high level during the period when the CLK pin is high; if CS# is pulled high during the period when HOLD# is low, the current operation will end.

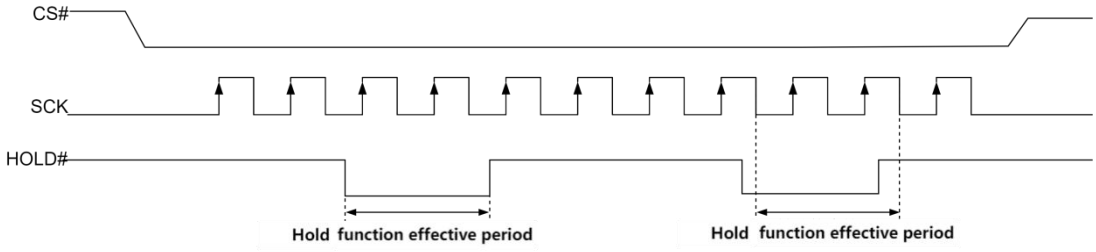


Figure 14: Hold function timing diagram

4.9 Reset Operation

The reset operation requires the execution of two command codes: reset enable command and reset command. After the user executes these two commands in sequence, the chip achieves the reset effect, and the values of all writable bits in the SR register become the default value 0. After a certain recovery time (t_{RST}), the chip can be read and written normally.

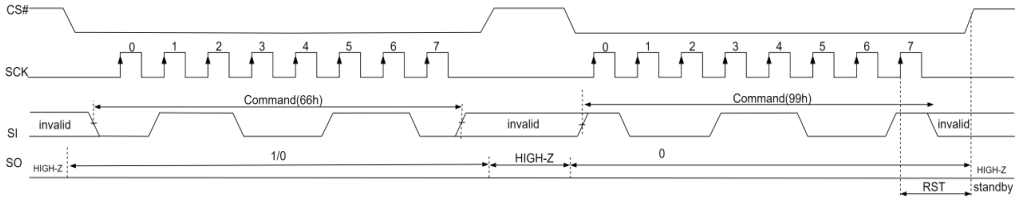


Figure 15: Reset Operation Timing

5 Chip Mode

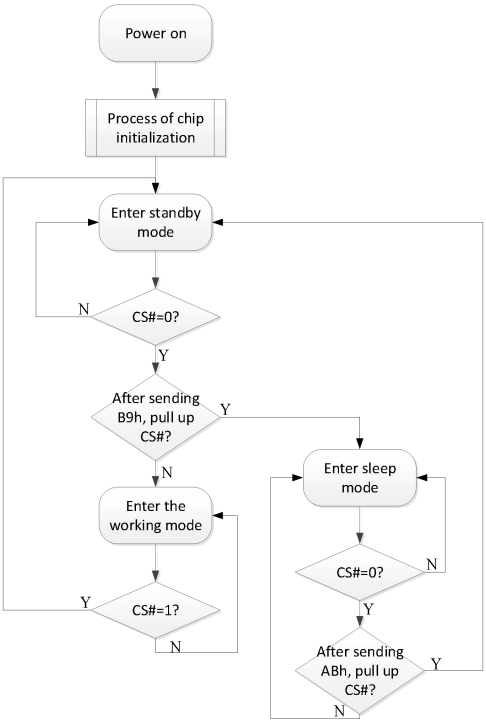


Figure 16: Chip mode switching

This chip provides 3 modes: working, standby, and sleep. In working mode, there are mainly read and write operations.

After power-on, when the chip initialization process is completed, the chip enters standby mode, the chip cannot receive command codes, the data in SI is invalid, and SO remains in High-Z state. Then when the user pulls down CS# and the command code sent is not B9h, the chip enters working mode, can receive the address and data on SI and read or write the data of the specified address according to the command code; when the user pulls down CS# and the command code sent is B9h, the chip will enter sleep mode. In this case, the internal power of the chip will be turned off and read and write operations cannot be performed. In working mode, when the user pulls up CS#, the chip returns to standby mode. In sleep mode, when the user pulls down CS# and issues an exit sleep mode command (ie ABh), the chip will perform a wake-up operation, restart the internal power, and switch from sleep mode to standby mode.

5.1 Entering Sleep Mode

Sleep mode is a low power mode. After entering this mode, the internal power of the chip is turned off to save power. The user can issue a sleep mode command (B9h), and the chip enters this mode after a certain period of time (TDP). If the power is cut off in sleep mode, the chip enters the normal standby state after the power is restored.

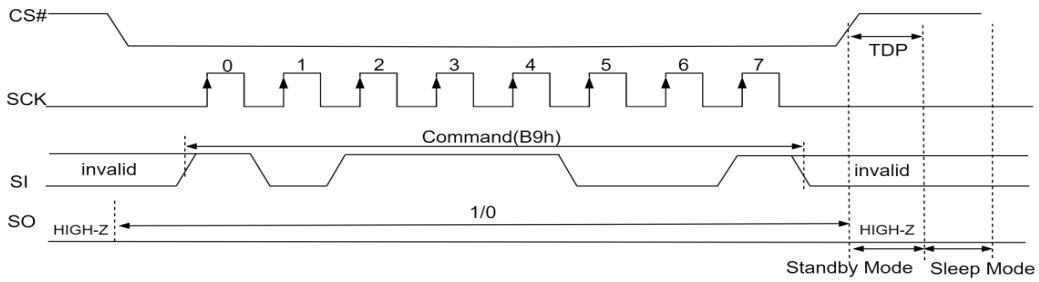


Figure 17: Enter sleep mode timing diagram

5.2 Exit Sleep Mode

When the chip is in sleep mode, the user can issue an exit sleep mode command (ABh) to make the chip enter the wake-up process. During the wake-up process, the internal power module will be turned on again. After the wake-up process is completed, the chip enters standby mode. The wake-up process takes TRDP.

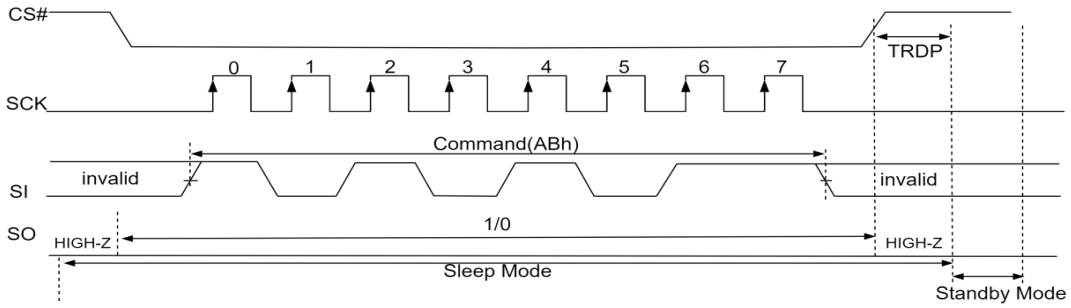


Figure 18: Exit sleep mode timing diagram

6 Absolute Maximum Ratings

Table 7: Absolute Maximum working conditions

Symbol	Parameter	Test Conditions	Value	Unit
VCC	Voltage Supply		-0.3 to 4	V
Vin	Voltage on any pin		0 to 3.6	V
Iout	Output current per pin		±20	mA
Tbias	Temperature under bias		-40 to 85	℃
Tstg	Storage Temperature		-55 to 125	℃
Tlead	Lead temperature during solder(3mins max)		260	℃
Hmax write	Maximum magnetic field during write*1	Write	12,000	A/m
Hmax read	Maximum magnetic field during read or standby*1	Read or Standby	12,000	A/m
Hmax power off	Maximum magnetic field during power off*1	Power off	45,000	A/m

Note: 1. The test conditions are room temperature and exposure to vertical magnetic field for one month to measure the anti-magnetic ability.

7 Electrical characteristics

This chapter introduces the electrical characteristics of the chip. The AC and DC parameter values shown in the following table are obtained based on the working conditions shown in Table 8 and the measurement conditions marked in Table 9. When users check a parameter, pay attention to matching the working conditions and measurement conditions.

7.1 Operating Conditions

Table 8: Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCC	Voltage Supply	2.7	3.3	3.6	V
Tax	Operating Temperature	-40		85	℃

7.2 DC characteristic

Table 9: DC characteristic

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_L	Input leakage current				±1	μA
I_{LO}	Output Leakage current				±1	μA

I_{SBY}	Standby current	CS#=HOLD#=VCC, WP#=SCK=SI=VSS		300	500	μA
I_{SLP}	Sleep Current	CS#=HOLD#=VCC, WP#=SCK=SI=VSS		2	4	μA
I_{CC1}	Write current	SPI@10MHz		3	5	mA
I_{CC2}	Read current	SPI@10MHz		3	5	mA
V_{IL}	Input low voltage		-0.3		0.2VCC	V
V_{IH}	Input high voltage		0.8VCC		VCC+0.3	V
V_{OL}	Output low voltage	I_{OL} = 4mA			0.5	V
V_{OH}	Output high level	I_{OH} = -4mA	VCC-0.6			V

7.3 AC Features

Table 13: AC Features

Symbol	Parameter	Min	Max	Unit
f_{SCK}	SCK clock frequency (normal read)		10	MHz
	SCK clock frequency (fast read)		20	
t_{WH}	Clock high time (except read operation)	15		ns
t_{WHR}	Clock high time (read operation)	20		ns
t_{WL}	Clock low time (except read operation)	15		ns
t_{WLR}	Clock low time (read operation)	20		ns
t_{CSS}	CS# setup time	3		ns
t_{CSH}	CS# hold time	10		ns
t_{SU}	Input data setup time on SCK rising edge	2		ns
t_H	Input data hold time on SCK rising edge	5		ns
t_V	Switch time from SCK falling edge to data valid	18	21	ns

t_{DIS}	CS# high to output data invalid time		6	ns
t_{OH}	Output data hold time on SCK falling edge	1.5		ns
t_{CS}	CS# high time (except write operation)	10		ns
t_{CSW}	CS# high time (write operation)	10		ns
t_{SH}	HOLD# setup time	10		ns
t_{HH}	HOLD# hold time	10		ns
t_{HHZ}	HOLD# low to output Hi-Z time	-	20	ns
t_{HLZ}	HOLD# high to output valid time	-	20	ns
t_{RST}	Reset recovery (normal reading and writing) time	600		μs
TDP	Enter sleep mode time		3	μs
TRDP	Exit sleep mode time		30	μs

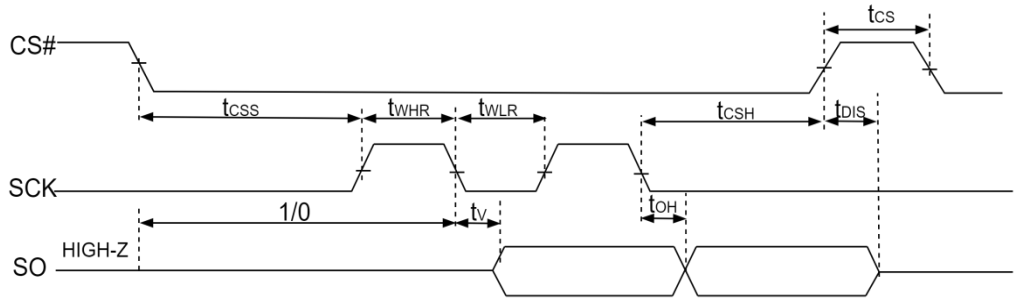


Figure 19: Normal read timing diagram

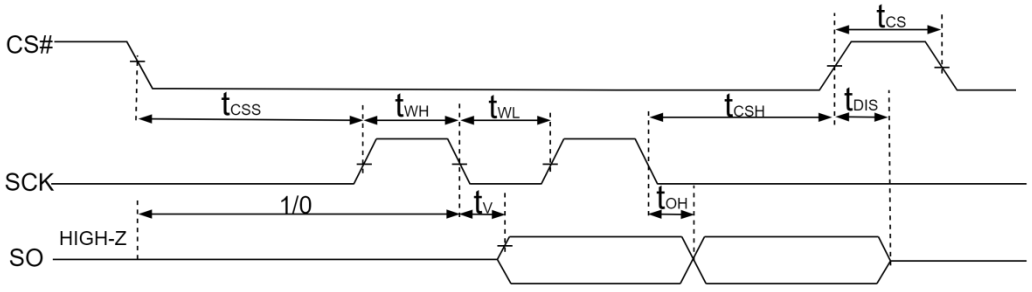


Figure 20: Fast read timing diagram

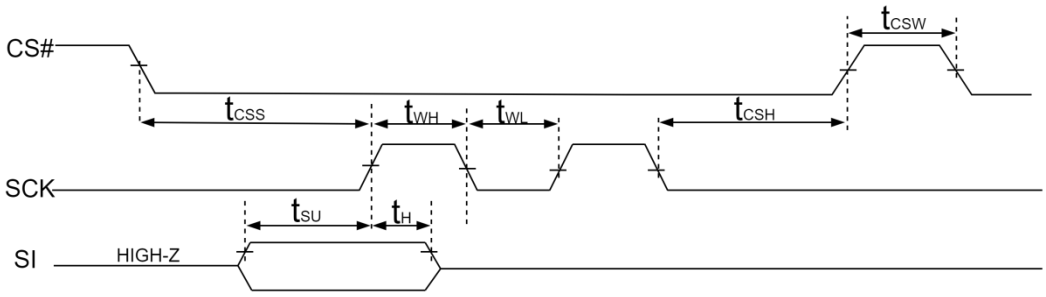


Figure 21: Input interface timing diagram

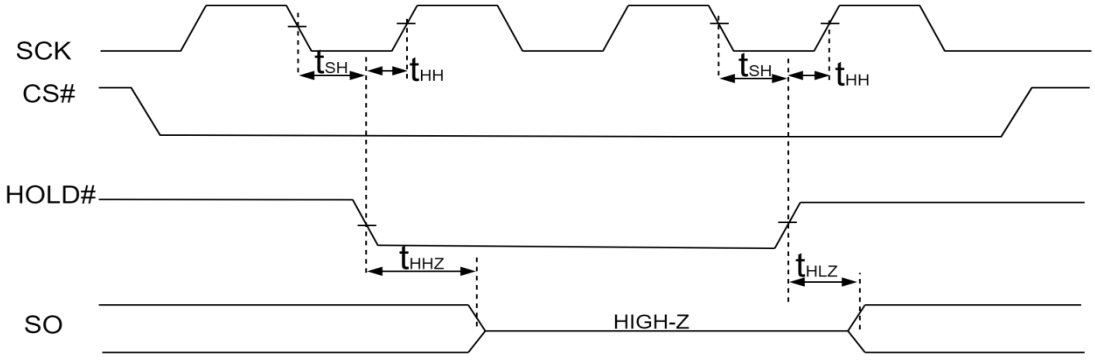


Figure 22: HOLD# interface timing diagram 1

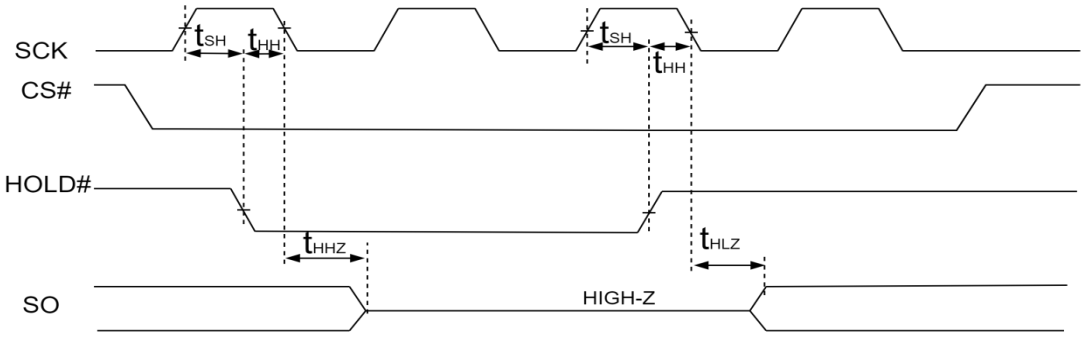


Figure 23: HOLD# interface timing diagram 2

7.4 Pin capacitance

Table 11: Pin capacitance

Symbol	Parameter	Max	Unit
C_{IN}	Control input capacitance	8	pF
C_{IO}	IO capacitance	12	pF
C_{LOAD}	Load Capacitance	32	pF

7.5 Power-on/Power-off Characteristics

In order to protect data during power-on, the chip does not support read or write operations when VCC is lower than VCC(min); VCC(min) refers to the minimum VCC value specified

when the chip is working normally, which is 2.7V in this chip, and VCC(max) refers to the maximum VCC value specified when the chip is working normally, which is 3.6V in this chip.

During the power-on, must wait for t_{PU} time (power-on delay time) after the voltage rises to VCC(min) before the chip can start working normally. This time is used to ensure that the internal voltage of the chip has stabilized. t_{PU} is measured from the time VCC reaches VCC(min).

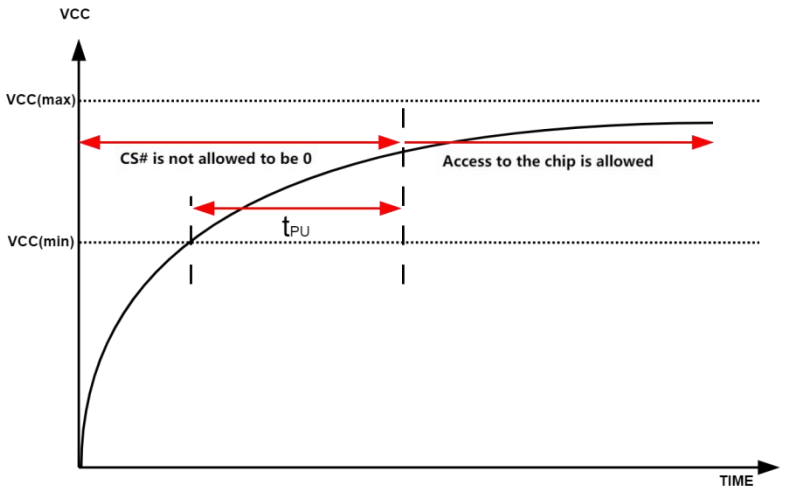


Figure 24: Power-on process diagram

At power-on, in order to properly initialize the chip, the following steps need to be performed:

(1) Reduce VCC power-up time (after t_{RVR} time).

(2) During power-on, CS# must follow VCC (a 10KΩ pull-up resistor to VCC is recommended).

(3) When VCC is lower than VCC(min), it is recommended not to send instructions to the chip.

(4) During the power-on, it is necessary to wait for t_{pu} before accessing.

(5) After power-on, the chip is in standby mode.

When the chip is powered off or out of power, please follow the following steps to properly shut down the device:

(1) Reduce VCC to below VCC_RST.

(2) During power-off, CS# must follow VCC (a 10KΩ pull-up resistor to VCC is recommended).

(3) When VCC is lower than VCC(min), it is not allowed to send instructions to the chip.

(4) After power-off, when VCC rises to above VCC(min), it is necessary to follow the power-on initialization process.

(5) In order to stabilize VCC, it is recommended to add a suitable decoupling capacitor to the VCC pin.

(6) If VCC rises from a voltage between VCC_ RST and VCC(min) to VCC, the chip is not guaranteed to work properly.

Table 12: Chip power-on/power-off parameters

Symbol	Parameter	Min	Max	Unit
t_{PU}	Power Up delay time	100	-	μs

t_{RVR}	Rise time from VCC to VCC(min)	-	30	ms
t_{RVF}	Falling time from VCC to VCC_RST	20	-	us
VCC_RST	VCC reset voltage	0	2	V
t_{PLOW}	VCC low level time	50	-	ms

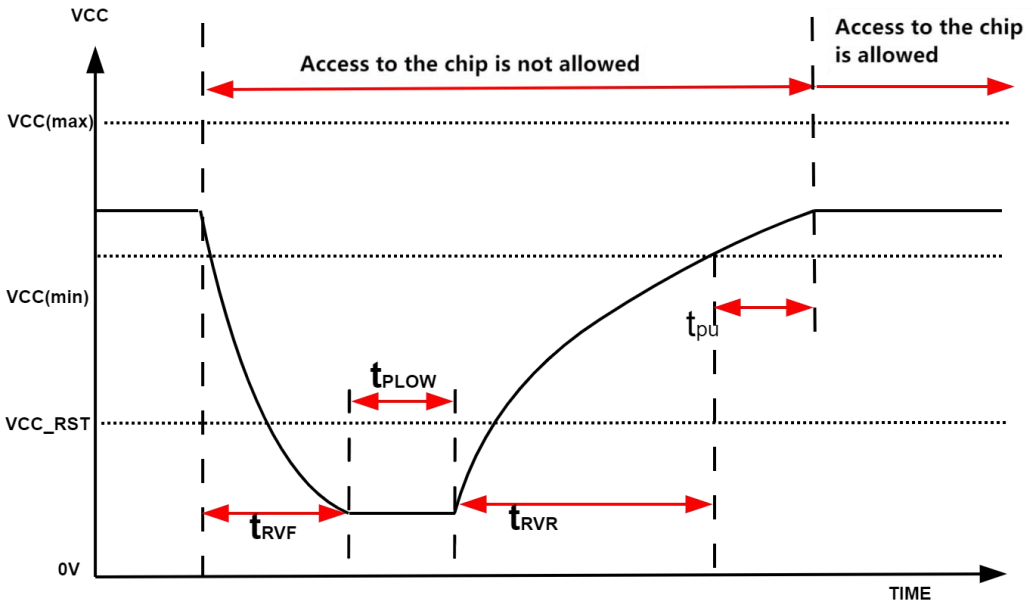
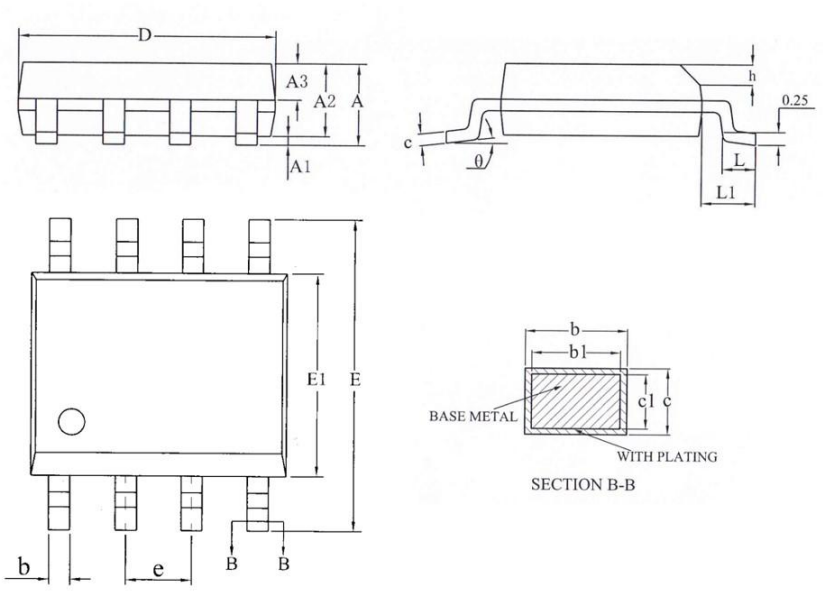


Figure 25: Power-off and power-on process diagram

8 Usage Notes

We recommend users to program the chip after reflow, because we cannot guarantee that the data written before reflow will still be valid after reflow.

9 Package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 26: SOP8 Package Outline

Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version: V1.0	Author: Zhao	Time: 2025.03

Modify the record:

1. First Edition

Statement

The information in the usage specification is correct at the time of publication, Shanghai Siproin Microelectronics Co.,Ltd. has the right to change and interpret the specification, and reserves the right to modify the product without prior notice. Users can obtain the latest version information from our official website or other effective channels before confirmation, and verify whether the relevant information is complete and up to date.

With any semiconductor product, there is a certain possibility of failure or failure under certain conditions. The buyer is responsible for complying with safety standards and taking safety measures when using the product for system design and complete machine manufacturing. The product is not authorized to be used as a critical component in life-saving or life-sustaining products or systems, in order to avoid potential failure risks that may cause personal injury or property loss.