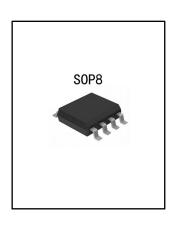


CMOS Leakage Current Protector A type

SSP54123A

General Description

The SSP54123A is a CMOS high-performance leakage protection integrated circuit. It encompasses a voltage regulator, an amplifier circuit, a comparison circuit, a delay circuit, a self-recovery control circuit, a latch controller, and an SCR drive circuit. This configuration allows it to effectively detect both AC leakage and DC pulsating leakage. It is primarily utilized in Type A leakage protectors.



Features

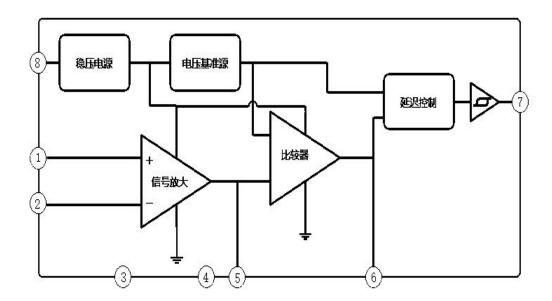
- When there is a leakage signal, the OUT output pulse width is greater than 20ms and can directly drive the SCR
- Used to detect A-type (including AC-type) leakage signals
- Various types of leakage signal tripping accuracy consistency is good
- Strong anti-electromagnetic interference (EMC) capability
- Applicable to AC voltage of 50Hz~60Hz, also applicable to DC voltage
- Wide operating temperature range (-20 \sim +85 °C)

Order Information

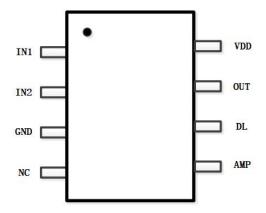
Part No	Package	Manner of Packing	Devices per reel
SSP54123A	SOP8	Reel	2500PCS



Block Diagram



Pin Arrangement Diagram and Pin Assignment



Pin No.	Pin Name	Description			
1	IN1	Amplifier input 1			
2	IN2	Amplifier input 2			
3	GND	Ground			
4	NC	No connection			
5	AMP	Internal amplifier output, external filter capacitor			
6	DL	Delay adjustment, external capacitor			
7	OUT	Trip signal output			
8	VDD	Power supply			



Functional Description

The SSP54123A leakage protector is a specialized integrated circuit designed to detect leakage currents on both the Live wire and Neutral wire. When a leakage current occurs, the Zero-Sequence Current Transformer (ZCT) senses this leakage and the secondary coil of the ZCT produces an output current. This output current serves as the input signal for the leakage protector chip. The leakage current may be in the form of DC, AC, or pulsating DC, which includes leakage signals at 0°, 90°, and 135° phase angles. If the Root Mean Square (RMS) value of the leakage current exceeds the rated current threshold specified by the leakage protector, the chip's output pin, labeled OUT, will trigger an action signal. The duration of this signal, or pulse width, will be greater than 20ms.

Absolute Maximum Ratings

Unless otherwise specified, T_{amb}= 25°C

Davamatar	Value	Unit	
Parameter	Min	Min Max	
Operating Temperature	-20	+85	°C
Storage Temperature	-55	+150	°C
Voltage at any pin to ground	-0.8	+6.5	V
Operating voltage	/	8.0	V
Operating current	/	8.0	mA

Electrical Characteristics

Unless otherwise specified, Tamb= 25°C

			Test	Recommended Value			
Parameter	Parameter Symbol Conditions		Circuits	Min	Тур	Max	Unit
Supply Current	I1	V _S =5V	1	/	/	2.6	mA
Supply Voltage	Vdd	V _S =5V	2	4.7	4.8	4.9	V
PIN6	13	Vs=5.5V,	3	50	/	68	μΑ
Output high current	15	Vin1-Vin2=30mV	3	50			
PIN6	I4	Vs=5.5V,	4	0.6	/	1.2	μΑ
Output low current	14	Vin1~Vin2 shorted	4				
PIN7 Output high curren	I7	Vs=5.5V, Vin1-Vin2=30mV	5	2.0	/	2.5	mA
PIN7 Output low level	Vo	Vs=5.5V,Vin1~Vin2 Short circuit, I6=50mA	6	/	/	0.2	V
Positive operating voltage	V+	Vs=5.5V,Vin1-Vin2 (Note 1)	7	4.5	5.1	5.7	mV
Negative operating voltage	V-	Vs=5.5V,Vin1-Vin2 (Note 1)	8	4.5	5.1	5.7	mV
Latching time	TON	Vs=5.5V,	9	20	/	/	ms



SSP54123A

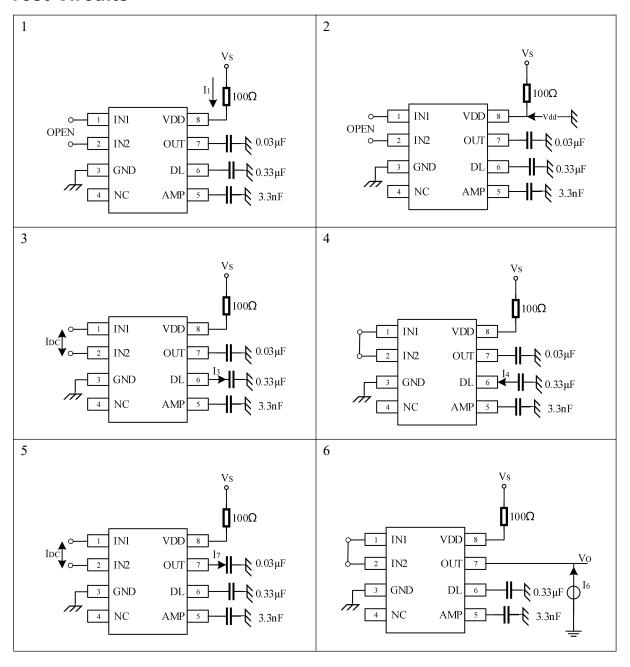
	Vin1-Vin2=30mV(Note			
	2)			

 $Note \ 1: When \ the \ DC \ voltage \ V+/V- \ between \ Vin1 \ and \ Vin2 \ is \ less \ than \ 4.5mV, \ the \ OUT \ pin \ outputs \ a \ low \ level.$

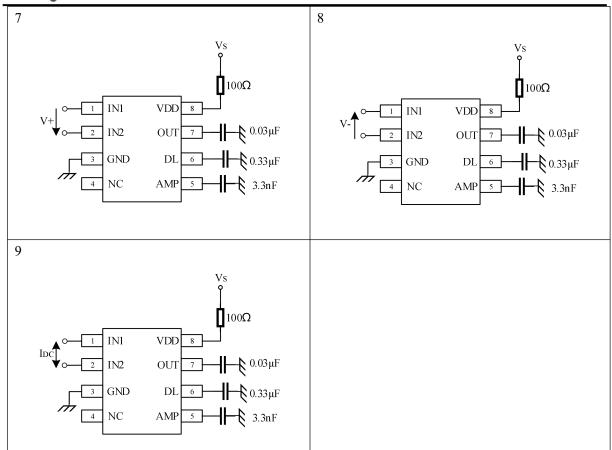
When V+/V- is greater than 5.7mV, the OUT pin outputs a high level.

Note 2: TON is the duration of OUT output high level.

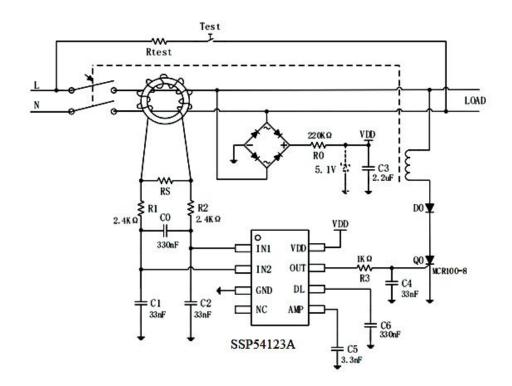
Test Circuits





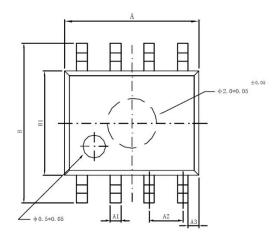


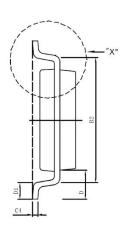
Application Circuits



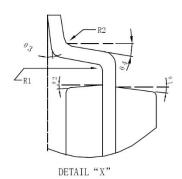


Package Information (SOP8)









Symbol	Min. (mm)	Max (mm)	Symbol	Min (mm)	Max (mm)	
A	4.95	5.15	C3	0.10	0.20	
A1	0.37	0.47	C4	0.20TYP		
A2	1.27T	ΥP	D	1.057	ГҮР	
A3	0.41T	ΥP	D1	0.50TYP		
В	5.80	6.20	R1	0.07TYP		
B1	3.80	4.00	R2	0.07TYP		
B2	5.0T	YP	θ1	17°TYP		
С	1.30	1.50	θ2	13°TYP		
C1	0.55	0.65	θ3	4°TYP		
C2	0.55	0.65	θ4	12°TYP		



Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version: V1.0 Author: Yang Time: 2023.04.26

Modify the record:

1. First promulgation

Statement

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