Low-Power, Sigma-Delta ADC with PGA and Reference

SSP1120

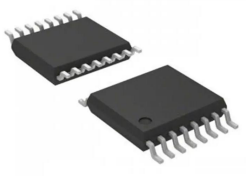
General Description

The SSP1120 is a precision, 16-bit, analog-to-digital converter (ADC) that offers many integrated features to reduce system cost and component count in applications measuring small sensor signals.

The device can perform conversions at data rates up to 2000 samples-per-second (SPS) with single-cycle settling. At 20 SPS, the digital filter offers simultaneous 50-Hz and 60-Hz rejection for noisy industrial applications. The internal PGA offers gains up to 128 V/V. This PGA makes the SSP1120 ideally suited for applications measuring small sensor signals, such as resistance temperature detectors (RTDs), thermocouples, thermistors, and bridge sensors.

Power consumption is as low as 120 µA@3.3V when operating in duty-cycle mode with the PGA disabled.

The SSP1120 is offered in a TSSOP-16 package and is specified over a temperature range of –40°C to +125°C.



TSSOP-16

Features

- Low Current Consumption:
  As Low as 120 µA (typ) in Duty-Cycle Mode@3.3V
- Wide Supply Range: 2.3 V to 5.5 V
- Programmable Gain: 1 V/V to 128 V/V
- Programmable Data Rates: Up to 2 kSPS
- 16-Bit Noise-Free Resolution at 20 SPS
- Simultaneous 50/60-Hz Rejection at 20 SPS with Single-Cycle Settling Digital Filter
- Two Differential or Four Single-Ended Inputs
- Dual-Matched Programmable Current Sources: 50 µA to 1.5 mA
- Internal 2.048-V Ref: 5 ppm/°C (typ) Drift
- Internal 2% Accurate Oscillator
- Internal Temperature Sensor: 1°C (typ)
- SPI-Compatible Interface(mode1)
- Package: TSSOP-16

APPLICATIONS

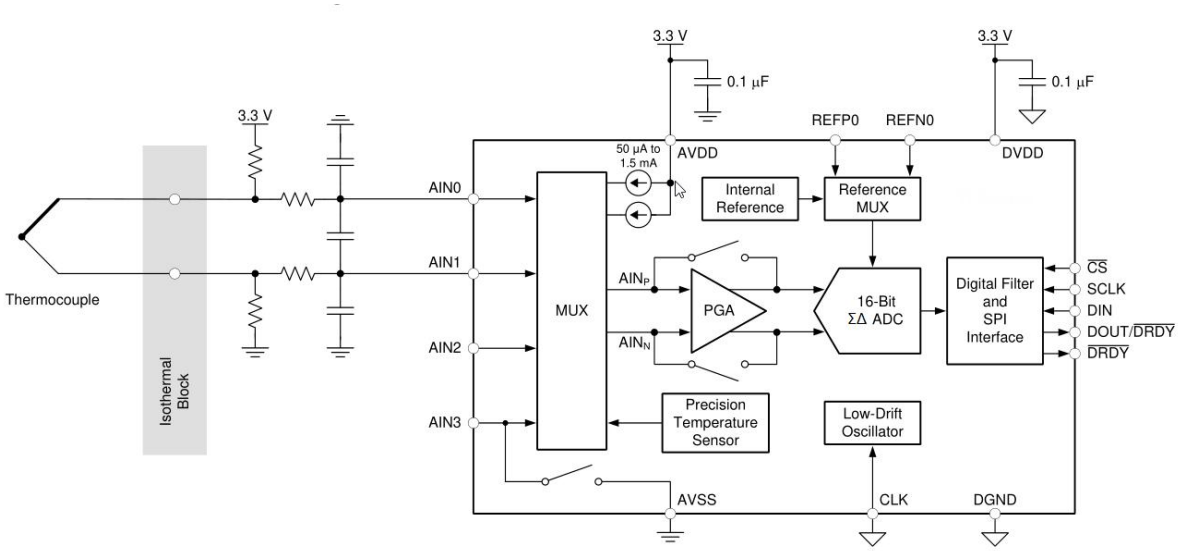
- Temperature Sensor Measurements:
  Thermistors/Thermocouples/Resistance
  Temperature Detectors (RTDs): 2-, 3-, or 4-Wire Types
- Resistive Bridge Sensor Measurements:
  Pressure Sensors/Strain Gauges/Weigh Scales
- Portable Instrumentation
- Factory Automation and Process Controls

Order Information

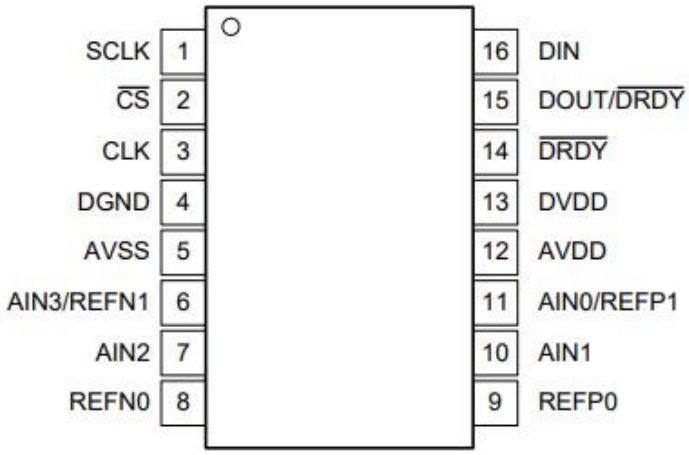
Ordering Name	Package	Manner of Packing	Minimum packing quantity
SSP1120	TSSOP-16	Reel	4000

Block Diagram and Pin Arrangement Diagram

K-Type Thermocouple Measurement



Pin Assignment



NAME	NO	IO	Description
AIN0/REFP1	11	Analog input	Analog input 0, positive reference input 1
AIN1	10	Analog input	Analog input 1
AIN2	7	Analog input	Analog input 2
AIN3/REFN1	6	Analog input	Analog input 3, negative reference input 1. Internal low-side power switch connected between AIN3/REFN1 and AVSS.
AVDD	12	Analog	Positive analog power supply
AVSS	5	Analog	Negative analog power supply
CLK	3	Digital input	External clock source pin. Connect to DGND if not used.
$\overline{CS}$	2	Digital input	Chip select; active low. Connect to DGND if not used.
DGND	4	Digital	Digital ground
DIN	16	Digital input	Serial data input
DOUT/$\overline{DRDY}$	15	Digital output	Serial data output; combined with data ready,active low
$\overline{DRDY}$	14	Digital output	Data ready, active low. Leave unconnected or tie to DVDD using a weak pull-up resistor if not used.
DVDD	13	Digital	Positive digital power supply
REFN0	8	Analog input	Negative reference input 0
REFP0	9	Analog input	Positive reference input 0
SCLK	1	Digital input	Serial clock input

Absolute Maximum Ratings(1)

Parameter		Min	Max	Unit
Power-supply voltage	AVDD to AVSS	-0.3	7	V
	DVDD to DGND	-0.3	7	V
	AVSS to DGND	–2.8	0.3	V
Analog input voltage	AIN0/REFP1, AIN1, AIN2, AIN3/REFN1, REFP0, REFN0	AVSS-0.3	AVDD+0.3	V
Digital input voltage	$\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, CLK	DGND-0.3	DVDD+0.3	V
Input current	Continuous, any pin except power supply pins	-10	10	mA
Temperature	Junction, T_J	-40	150	℃
	Storage, T_{stg}	-60	150	℃

Note (1): Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter		Min	Typ	Max	Unit
POWER SUPPLY					
Unipolar analog power supply	AVDD to AVSS	2.3		5.5	V
	AVSS to DGND	-0.1	0	0.1	V
Bipolar analog power supply	AVDD to DGND	2.3	2.5	5.5	V
	AVSS to DGND	–2.75	–2.5	–2.3	V
Digital power supply	DVDD to DGND	2.3		5.5	V
VOLTAGE REFERENCE INPUTS					
V_{ref} Differential reference input voltage	$V_{ref} = V_{(REFPx)} - V_{(REFNx)}$	0.75	2.5	AVDD	V
$V_{(REFNx)}$ Absolute negative reference voltage		AVSS-0.1		$V_{(REFPx)}$-0.75	V
$V_{(REFPx)}$ Absolute positive reference voltage		$V_{(REFNx)}$+0.75		AVDD + 0.1	V
EXTERNAL CLOCK SOURCE					
$f_{(CLK)}$ External clock frequency		0.5	4.096	4.5	MHz
Duty cycle		40%		60%	
DIGITAL INPUTS					
Input voltage		DGND		DVDD	V
TEMPERATURE RANGE					
T_A Operating ambient temperature		-40		125	℃

Electrical Characteristics

Default Test Condition: Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. AVDD=DVDD=3.3V, AVSS=0V, PGA disabled, DR=20SPS, and external V_{ref}=2.048 V(unless otherwise noted).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM PERFORMANCE						
Resolution (no missing codes)			16			Bits
Data rate	DR	Normal mode	20, 45, 90, 175, 330, 600, 1000			SPS
		Duty-cycle mode	5, 11.25, 22.5, 44, 82.5, 150, 250			SPS
		Turbo mode	40, 90, 180, 350, 660, 1200, 2000			SPS
Noise (input-referred)			See the Noise Performance section			
Integral nonlinearity	INL	Gain=1 to 128, VCM=0.5*AVDD, best fit		20		ppm_{FSR}
Input offset voltage	VIO	PGA disabled, gain = 1 to 4, differential inputs		±2		µV
		Gain= 1 to 128, differential inputs		±2		µV
Offset drift		PGA disabled, gain = 1 to 4		0.1	0.3	µV/°C
		Gain= 1 to 128, T_A= –40°C to +85°C		0.1	0.3	µV/°C
		Gain = 1 to 128		0.3	0.5	µV/°C
Gain error		PGA disabled, gain = 1 to 4		0.2		%
		Gain = 1 to 128, T_A = 25°C	-0.5	±0.2	0.5	%
Gain drift		PGA disabled, gain = 1 to 4		5		ppm/°C
		Gain = 1 to 128		5	20	ppm/°C
Normal-mode rejection ratio	NMRR	50 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 10	105			dB
		60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 11	105			dB
		50 Hz or 60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 01	90			dB
Common-mode rejection ratio	CMRR	At dc, gain = 1	90	97		dB
		$f_{(CM)}$ = 50 Hz, DR = 2000 SPS		116		dB
		$f_{(CM)}$ = 60 Hz, DR = 2000 SPS		116		dB
Power-supply rejection ratio	PSRR	AVDD at dc, VCM= 0.5AVDD, gain= 1	80	105		dB
		DVDD at dc, VCM=0.5AVDD, gain=1	100	115		dB
INTERNAL VOLTAGE REFERENCE						
Initial accuracy		T_A = 25°C		2.048		V
Reference drift		-45~125°C		5	30	ppm/°C
		-45~85°C		4	10	ppm/°C

		0~85°C		3	7	ppm/°C
VOLTAGE REFERENCE INPUTS						
Reference input current		REFP0 = V_{ref}, REFN0 = AVSS		180		nA
INTERNAL OSCILLATOR						
Internal oscillator accuracy		Normal mode	-2	±1	2	%
EXCITATION CURRENT SOURCES (IDACs)						
Current settings			50, 100, 250, 500, 1000, 1500			µA
Compliance voltage		All current settings			AVDD – 0.9	V
Accuracy		All current settings, each IDAC	-6	±1	6	%
EXCITATION CURRENT SOURCES (IDACs)						
Current match		Between IDACs		±0.3		%
Temperature drift		Each IDAC		150		ppm/°C
Temperature drift matching		Between IDACs		20		ppm/°C
TEMPERATURE SENSOR						
Conversion resolution				14		Bits
Temperature resolution				0.03215		°C
Accuracy		T_A = 0°C to +75°C		±0.5		°C
		T_A = –40°C to +125°C		±1		°C
Accuracy vs analog supply voltage				0.1		°C/V
LOW-SIDE POWER SWITCH						
On-resistance	R_{ON}			3		Ω
Current through switch					30	mA
DIGITAL INPUTS/OUTPUTS						
High-level input voltage	V_{IH}		0.7DVDD		DVDD	V
Low-level input voltage	V_{IL}		DGND		0.3DVDD	V
High-level output voltage	V_{OH}	I_{OH} = 3 mA	0.8DVDD			V
Low-level output voltage	V_{OL}	I_{OL} = 3 mA			0.2DVDD	V

Input leakage, high	I_H	V_{IH} = 5.5 V	-10		10	μA
Input leakage, low	I_L	V_{IL} = DGND	-10		10	μA
POWER SUPPLY						
Analog supply current	I_{AVDD}	Power-down mode		0.05		μA
		Duty-cycle mode, PGA disabled		135		μA
		Duty-cycle mode, gain = 1 to 16		160		μA
		Duty-cycle mode, gain = 32		172		μA
		Duty-cycle mode, gain = 64, 128		182		μA
		Normal mode, PGA disabled		342		μA
		Normal mode, gain = 1 to 16		448		μA
		Normal mode, gain = 32		499		μA
		Normal mode, gain = 64, 128		550		μA
		Turbo mode, PGA disabled		402		μA
		Turbo mode, gain = 1 to 16		613		μA
		Turbo mode, gain = 32		715		μA
		Turbo mode, gain = 64, 128		817		μA
Digital supply current	I_{DVDD}	Power-down mode		1.3		μA
		Duty-cycle mode		44		μA
		Normal mode		43		μA
		Turbo mode		73		μA
POWER SUPPLY						
Power dissipation	P_D	Duty-cycle mode, PGA disabled		0.5907		mW
		Normal mode, gain = 1 to 16		1.6203		mW
		Turbo mode, gain = 1 to 16		2.2638		mW

Noise Performance

Sigma-delta (ΣΔ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΣΔ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called oversampling ratio (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

ENOB = ln (Full-Scale Range / $V_{RMS\text{-}Noise}$) / ln(2);

Noise-Free Bits = ln (Full-Scale Range / $V_{PP\text{-}Noise}$) / ln(2)

Full-Scale Range= 2 · V_{ref} / Gain;

DATA RATE	Noise in μVRMS (μVPP)
	GAIN (PGA Enabled)

(SPS)	1	2	4	8	16	32	64	128
20	62.5 (125)	31.25 (125)	29.38 (62.5)	30.63 (62.5)	28.75 (125)	23.13 (125)	25.63 (125)	38.75 (187.5)
45	62.5 (125)	31.25 (125)	27.5 (125)	27.5 (125)	21.25 (125)	23.75 (125)	25 (125)	31.88 (125)
90	62.5 (125)	31.25 (125)	32.5 (125)	21.25 (125)	30.63 (125)	25.63 (125)	33.75 (125)	48.13 (187.5)
175	62.5 (125)	31.25 (125)	33.75 (125)	29.38 (62.5)	32.5 (187.5)	32.5 (187.5)	40.63 (187.5)	68.75 (375)
330	62.5 (187.5)	31.88 (125)	34.38 (187.5)	30.63 (62.5)	33.13 (125)	41.25 (187.5)	43.13 (187.5)	75 (437.5)
600	62.5 (125)	45 (187.5)	48.13 (187.5)	30.63 (125)	44.38 (187.5)	51.88 (250)	61.88 (375)	100 (500)
1000	62.5 (187.5)	35.63 (125)	41.25 (250)	40 (187.5)	46.25 (250)	52.5 (250)	62.5 (375)	118.75 (687.5)

DATA RATE (SPS)	ENOB from RMS Noise (Noise-free Bits from Peak-to-Peak Noise) GAIN (PGA Enabled)							
	1	2	4	8	16	32	64	128
20	16(15)	16(15)	16(16)	16(16)	16(15)	16(15)	16(15)	16(14.42)
45	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)
90	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16(15)	16(14.42)
175	16(15)	16(15)	16(15)	16(16)	16(14.42)	16(14.42)	16(14.42)	15.86(13.42)
330	16(14.42)	16(15)	16(14.42)	16(16)	16(15)	16(14.42)	16(14.42)	15.74(13.19)
600	16(15)	16(14.42)	16(14.42)	16(15)	16(14.42)	16(14)	16(13.42)	15.32(13)
1000	16(14.42)	16(15)	16(14)	16(14.42)	16(14)	16(14)	16(13.42)	15.07(12.54)

DATA RATE (SPS)	Noise in μVRMS (μVPP) GAIN (PGA Disabled)		
	1	2	4
20	62.5(125)	31.25(125)	30(62.5)
45	62.5(62.5)	31.25(125)	26.88(62.5)
90	62.5(125)	31.25(62.5)	30.63(125)
175	62.5(125)	31.25(125)	31.25(62.5)
330	62.5(125)	31.25(125)	32.5(125)
600	62.5(187.5)	38.13(187.5)	32.5(187.5)
1000	62.5(187.5)	38.13(187.5)	39.38(187.5)

DATA RATE (SPS)	ENOB RMS Noise (Peak-to-Peak) GAIN (PGA Disabled)		
	1	2	4
20	16(15)	16(15)	16(16)
45	16(16)	16(15)	16(16)
90	16(15)	16(16)	16(15)
175	16(15)	16(15)	16(16)
330	16(15)	16(15)	16(15)
600	16(14.42)	16(14.42)	16(14.42)
1000	16(14.42)	16(14.42)	16(14.42)

SPI Timing Requirements

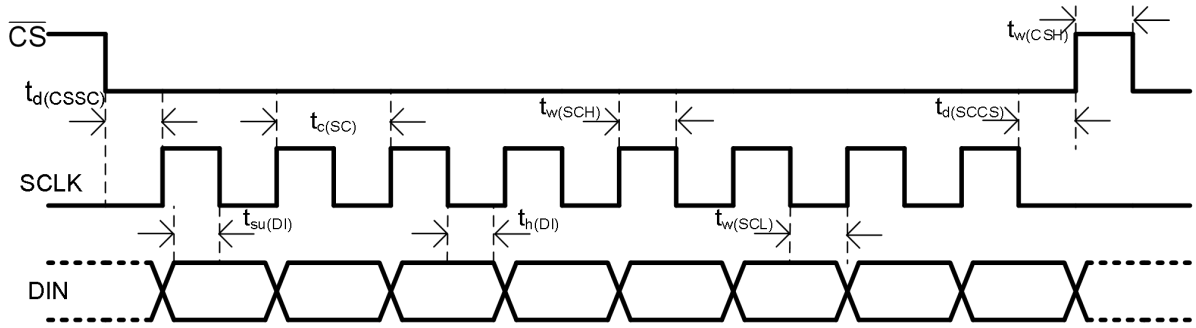
over operating ambient temperature range and DVDD = 2.3 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1)	50		ns
$t_{d(SCCS)}$	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge	25		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	50		ns
$t_{c(SC)}$	SCLK period	150		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	60		ns
$t_{w(SCL)}$	Pulse duration, SCLK low	60		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	50		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	25		ns
SPI timeout(2)	Normal mode, duty-cycle mode		13955	$t_{(MOD)}$
	Turbo mode		27910	$t_{(MOD)}$

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.

(2) $t_{(MOD)} = 1 / f_{(MOD)}$. Modulator frequency $f_{(MOD)}$ = 256 kHz (normal mode, duty-cycle mode) and 512 kHz (turbo mode), when using the internal oscillator or an external 4.096-MHz clock.

Serial Interface Timing Requirements

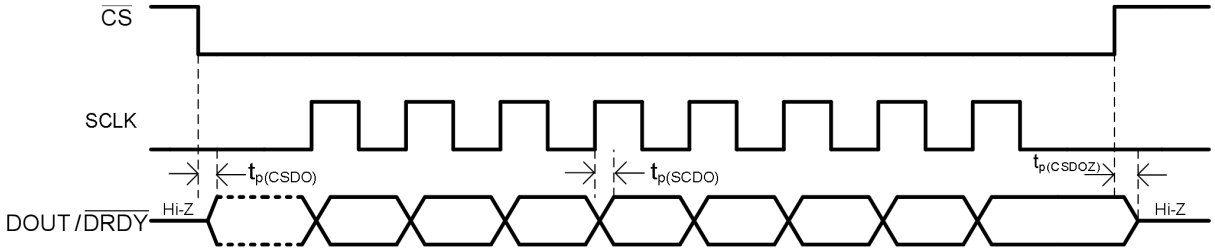


NOTE: Single-byte communication is shown. Actual communication may be multiple bytes.

SPI Switching Characteristics

over operating ambient temperature range and DVDD = 2.3 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time,$\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 10 kΩ to DGND		50	ns
$t_{p(SCDO)}$	Propagation delay time,SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 10 kΩ to DGND	0	25	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 10 kΩ to DGND		50	ns



NOTE: Single-byte communication is shown. Actual communication may be multiple bytes.

Register Map

The device has four 8-bit configuration registers that are accessible through the serial interface using the RREG and WREG commands. The configuration registers control how the device operates and can be changed at any time without causing data corruption. After power-up or reset, all registers are set to the default values (which are all 0). All registers retain their values during power-down mode. Under table shows the register map of the configuration registers.

Configuration Register Map

REGISTER (Hex)	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00h	MUX[3:0]				GAIN[2:0]			PGA_BYPASS
01h	DR[2:0]			MODE[1:0]		CM	TS	BCS
02h	VREF[1:0]		50/60[1:0]		PSW	IDAC[2:0]		
03h	I1MUX[2:0]			I2MUX[2:0]			DRDYM	0

Configuration Register 0(offset=00h) [reset=00h]

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
MUX[3:0]				GAIN[2:0]			PGA_BYPASS
R/W-0h				R/W-0h			R/W-0h

R/W = Read/Write; -n = value after reset

Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MUX[3:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. For settings where AIN_N = AVSS, the PGA must be disabled (PGA_BYPASS = 1) and only gains 1, 2, and 4 can be used. 0000 : AIN_P = AIN0, AIN_N = AIN1 (default) 0001 : AIN_P = AIN0, AIN_N = AIN2 0010 : AIN_P = AIN0, AIN_N = AIN3 0011 : AIN_P = AIN1, AIN_N = AIN2 0100 : AIN_P = AIN1, AIN_N = AIN3 0101 : AIN_P = AIN2, AIN_N = AIN3 0110 : AIN_P = AIN1, AIN_N = AIN0 0111 : AIN_P = AIN3, AIN_N = AIN2

				1000 : AIN_P = AIN0, AIN_N = AVSS 1001 : AIN_P = AIN1, AIN_N = AVSS 1010 : AIN_P = AIN2, AIN_N = AVSS 1011 : AIN_P = AIN3, AIN_N = AVSS 1100 : Reserved 1101 : (AVDD – AVSS) / 4 monitor (PGA bypassed) 1110 : AIN_P and AIN_N shorted to (AVDD + AVSS) / 2 1111 : Reserved
3:1	GAIN[2:0]	R/W	0h	**Gain configuration** These bits configure the device gain. Gains 1, 2 and 4 can be used without the PGA. In this case, gain is obtained by a switched-capacitor structure. 000 : Gain = 1 (default) 001 : Gain = 2 010 : Gain = 4 011 : Gain = 8 100 : Gain = 16 101 : Gain = 32 110 : Gain = 64 111 : Gain = 128
0	PGA_BYPASS	R/W	0h	**Disables and bypasses the internal low-noise PGA** Disabling the PGA reduces overall power consumption and allows the commonmode voltage range (V_{CM}) to span from AVSS – 0.1 V to AVDD + 0.1 V. The PGA can only be disabled for gains 1, 2, and 4. The PGA is always enabled for gain settings 8 to 128, regardless of the PGA_BYPASS setting. 0 : PGA enabled (default) 1 : PGA disabled and bypassed

Configuration Register 1(offset=01h) [reset=00h]

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
DR[2:0]			MODE[1:0]		CM	TS	BCS
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h

R/W = Read/Write; -n = value after reset

Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DR[2:0]	R/W	0h	**Data rate** These bits control the data rate setting depending on the selected operating mode. Next table lists the bit settings for normal, duty-cycle, and turbo mode.

4:3	MODE[1:0]	R/W	0h	**Operating mode** These bits control the operating mode the device operates in. 00 : Normal mode (256-kHz modulator clock, default) 01 : Duty-cycle mode (internal duty cycle of 1:4) 10 : Turbo mode (512-kHz modulator clock) 11 : Reserved
2	CM	R/W	0h	**Conversion mode** This bit sets the conversion mode for the device. 0 : Single-shot mode (default) 1 : Continuous conversion mode
1	TS	R/W	0h	**Temperature sensor mode** This bit enables the internal temperature sensor and puts the device in temperature sensor mode. The settings of configuration register 0 have no effect and need use the internal reference for measurement when temperature sensor mode is enabled. 0 : Disables temperature sensor (default) 1 : Enables temperature sensor
0	BCS	R/W	0h	**Burn-out current sources** This bit controls the 10-µA, burn-out current sources. The burn-out current sources can be used to detect sensor faults such as wire breaks and shorted sensors. 0 : Current sources off (default) 1 : Current sources on

DR Bit Settings(1)

NORMAL MODE	DUTY-CYCLE MODE	TURBO MODE
000=20SPS	000=5SPS	000=40SPS
001=45SPS	001=11.25SPS	001=90SPS
010=90SPS	010=22.5SPS	010=180SPS
011=175SPS	011=44SPS	011=350SPS
100=330SPS	100=82.5SPS	100=660SPS
101=600SPS	101=150SPS	101=1200SPS
110=1000SPS	110=250SPS	110=2000SPS
111=Reserved	111=Reserved	111=Reserved

Note(1):Data rates provided are calculated using the internal oscillator or an external 4.096-MHz clock. The data rates scale proportionally with the external clock frequency when an external clock other than 4.096 MHz is used.

Configuration Register 2(offset=02h) [reset=00h]

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
VREF[1:0]		50/60[1:0]		PSW	IDAC[2:0]		
R/W-0h		R/W-0h		R/W-0h	R/W-0h		

R/W = Read/Write; -n = value after reset

Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	VREF[1:0]	R/W	0h	**Voltage reference selection** These bits select the voltage reference source that is used for the conversion. 00 : Internal 2.048-V reference selected (default) 01 : External reference selected using dedicated REFP0 and REFN0 inputs 10 : External reference selected using AIN0/REFP1 and AIN3/REFN1 inputs 11 : Analog supply (AVDD – AVSS) used as reference
5:4	50/60[1:0]	R/W	0h	**FIR filter configuration** These bits configure the filter coefficients for the internal FIR filter. Only use these bits together with the 20-SPS setting in normal mode and the 5 SPS setting in duty-cycle mode. Set to 00 for all other data rates. 00 : No 50-Hz or 60-Hz rejection (default) 01 : Simultaneous 50-Hz and 60-Hz rejection 10 : 50-Hz rejection only 11 : 60-Hz rejection only
3	PSW	R/W	0h	**Low-side power switch configuration** This bit configures the behavior of the low-side switch connected between AIN3/REFN1 and AVSS. 0 : Switch is always open (default) 1 : Switch automatically closes when the START/SYNC command is sent and opens when the POWERDOWN command is issued.
2:0	IDAC[2:0]	R/W	0h	**IDAC current setting** These bits set the current for both IDAC1 and IDAC2 excitation current sources. 000 : Off (default) 001 : Reserved 010 : 50 µA 011 : 100 µA 100 : 250 µA

				101 : 500 µA 110 : 1000 µA 111 : 1500 µA

Configuration Register 3(offset=03h) [reset=00h]

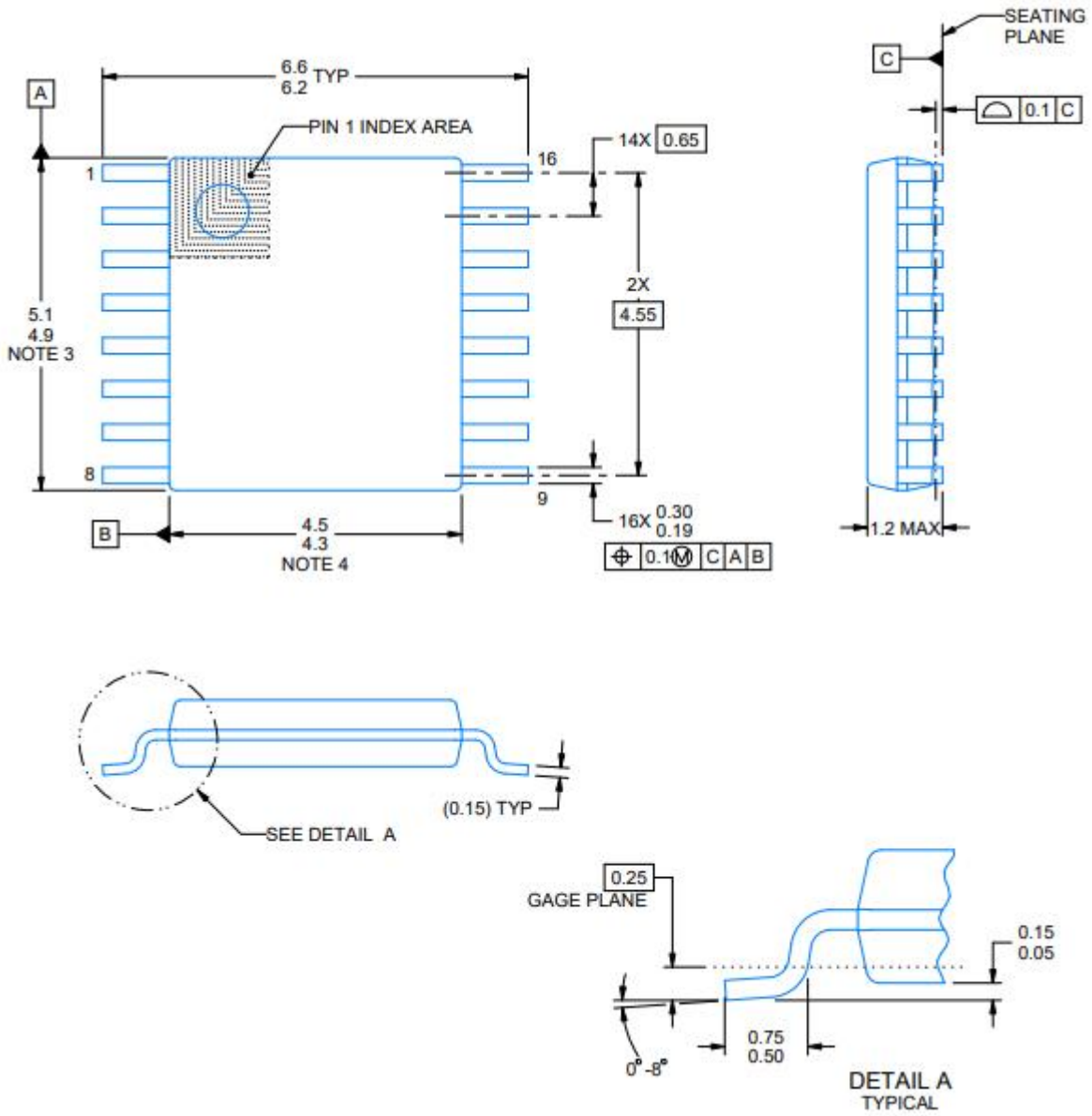
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
I1MUX[2:0]			I2MUX[2:0]			DRDYM	0
R/W-0h			R/W-0h			R/W-0h	R/W-0h

R/W = Read/Write; -n = value after reset

Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	I1MUX[2:0]	R/W	0h	**IDAC1 routing configuration** These bits select the channel where IDAC1 is routed to. 000 : IDAC1 disabled (default) 001 : IDAC1 connected to AIN0/REFP1 010 : IDAC1 connected to AIN1 011 : IDAC1 connected to AIN2 100 : IDAC1 connected to AIN3/REFN1 101 : IDAC1 connected to REFP0 110 : IDAC1 connected to REFN0 111 : Reserved
4:2	I2MUX[2:0]	R/W	0h	**IDAC2 routing configuration** These bits select the channel where IDAC2 is routed to. 000 : IDAC2 disabled (default) 001 : IDAC2 connected to AIN0/REFP1 010 : IDAC2 connected to AIN1 011 : IDAC2 connected to AIN2 100 : IDAC2 connected to AIN3/REFN1 101 : IDAC2 connected to REFP0 110 : IDAC2 connected to REFN0 111 : Reserved
1	DRDYM	R/W	0h	**$\overline{\text{DRDY}}$ mode** This bit controls the behavior of the DOUT/$\overline{\text{DRDY}}$ pin when new data are ready. 0 : Only the dedicated $\overline{\text{DRDY}}$ pin is used to indicate when data are ready (default). 1 : Data ready is indicated simultaneously on DOUT/$\overline{\text{DRDY}}$ and $\overline{\text{DRDY}}$.
0	Reserved	R/W	0h	**Reserved** Always write 0

Package Information（TSSOP16）



Special Instructions

The company reserves the right of final interpretation of this specification.

Version Change Description

Version：V1.0	Author：Yang	Time：2023.8.29
Modify the record：		
1. Editio princeps		
Version：V1.01	Author：Yang	Time：2024.1.16
Modify the record：		
1. Modify the correlation description of ΣΔ		
2. Modify the Features parameters		
3. Modify the Order Information		
4. Modify the Absolute Maximum Ratings parameters		
5. Modify the Register Map contents		

Statement

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